Single-electron charging phenomena in silicon nanopillars with and without silicon nitride tunnel barriers

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Electron transport in silicon nanopillars has been studied for pillars with zero, one, or two silicon nitride barrier layers of 2 nm thickness. Evidence of Coulomb blockade is presented and the role of the silicon nitride layers is discussed. Wide zero current regions are observed for some devices with two silicon nitride tunnel barriers and these are attributed to the formation of fully depleted quantum dots. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1405825]

I. INTRODUCTION

Recent developments in vertical transistor structures have produced devices with the potential for scaling down to the nanometer regime.[1,2] Coulomb blockade effects are likely to become important as devices are scaled down and these have also generated a great deal of interest recently because of potential applications in new devices. The use of vertical Coulomb blockade structures makes it possible to use well-defined islands and barriers[3] and experiments on GaAs-based heterostructures have shown Coulomb blockade oscillations as individual electrons are added to a quantum dot.[4] The higher barrier heights in similar silicon structures give them the potential to operate at much higher temperatures. Fukuda *et al.*[5] demonstrated that ultrathin Si_3N_4 barriers can be formed in silicon pillars. We have fabricated nanopillars with and without silicon nitride layers in phosphorus-doped polycrystalline silicon (polysilicon) and studied the electron transport in such pillars with a view to understanding the role of nitride layers in controlling single-electron charging effects.

II. MATERIAL AND FABRICATION

Details of wafer growth and pillar fabrication are published elsewhere[6] but an outline of the fabrication process is given here. Alternating layers of polysilicon and silicon nitride (Si_3N_4) were grown by low pressure chemical vapor deposition using silane (SiH_4) and phosphine (PH_3) and heating to 900 °C in ammonia (NH_3) without breaking vacuum which produces a self-limiting 2 nm thick silicon nitride layer. Rapid thermal annealing at 900 °C for 30 s was used to activate the dopant atoms in the final polysilicon layer. The concentration of active dopant atoms was about $3\times10^{18}\,cm^{-3}$ at 20 K. Figure 1 shows a bright-field transmission electron micrograph of a typical section of the two-barrier wafer used here. The nitride layers are labeled A and B. The nitride barriers are separated by 20 nm of relatively fine-grained polysilicon with grain sizes ranging from 5 to 20 nm. Outside the barriers the polysilicon grains are coarser and are predominantly columnar in structure. The upper and lower silicon nitride barriers are approximately 1.6 and 2.0 nm thick, respectively.

A schematic of the device structure is shown in Fig. 2. The pillars are defined using high-resolution electron beam lithography followed by evaporation of 60/40 Pd/Au and lift-off to form the top contact. Reactive ion etching using a combination of $SiCl_4$ and CF_4 was used to provide a highly anisotropic etch which formed pillars with almost vertical sidewalls. The metal was then removed in aqua regia (3:1 HCl:HNO_3). Some of the pillars were oxidized in a dry oxygen furnace at 1000 °C, producing a 30 nm thick oxide layer. Planarization of the pillars was performed by spin coating and curing a polyamide film and etching back to the pillar tops so that electrical contacts can be made to the top of the pillar. Difficulties in making a good top contact to the oxidized devices without overetching the oxide resulted in a low device yield, so most of the results presented are for unoxidized devices. We present a comparison of conduction characteristics for pillars of different diameters and with between zero and two silicon nitride barriers.

III. RESULTS AND DISCUSSION

The bonding process used in previous experiments[7] often damaged the devices and altered their $I-V$ characteristics and, in order to avoid this, the measurements presented here are from devices measured using a BCT-43MDC cryogenic prober from Nagase & Co. Ltd. with a base sample temperature of about 20 K and a Hewlett-Packard 4156A parameter analyzer.

Different types of confinement are important for the different layer structures. Lateral confinement from the surface potential leads to a depletion region and gives an effective channel diameter around 50 nm smaller than the pillar diameter. This is important for all the different layer structures.

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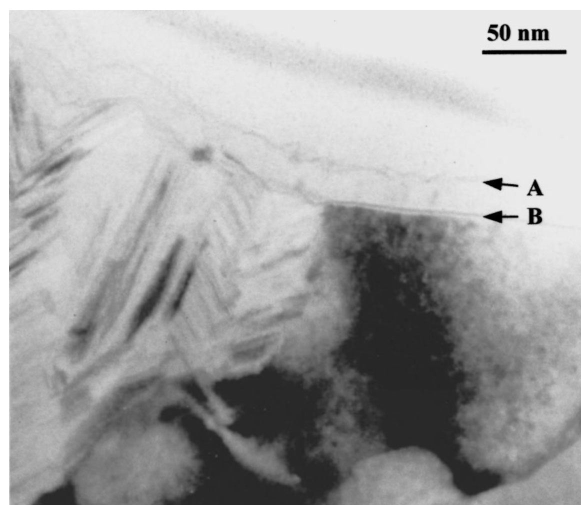

FIG. 1. Bright-field tunneling electron micrograph of the double-barrier wafer showing silicon nitride tunnel barriers A and B.

Potential fluctuations due to random placement of dopant atoms are typically 200 meV or lower[8] and are most important for the smallest conducting pillars (<65 nm diameter). Grain boundaries are important and produce potential barriers typically less than 100 meV in height.[9] These are present in all devices except in the case of single-crystal zero-barrier nanopillars but may have an increased effect for the fine-grained structure between the nitride barriers in the double-barrier system. The silicon nitride layers produce barriers around 1.9 eV in height.[10]

A. Devices without silicon nitride barriers

Both single-crystal and polycrystalline nanopillars without silicon nitride barriers were fabricated and most of these did not show any strong nonlinearity at 20 K. However, a fraction of these, depending on the pillar dimensions, exhibited Coulomb blockade behavior with Coulomb gaps ranging from 25 to 80 mV in size. Having characterized many samples, we estimate that polysilicon nanopillars 400 nm in height with diameters of 50 ± 5 nm had a 40% probability of showing a zero current region at 20 K with the probability dropping off rapidly to 10% for 65 ± 5 nm diam pillars. For single-crystal nanopillars, the probability of observing Coulomb blockade dropped off more rapidly with increasing pillar diameter, although there were not enough devices to be statistically certain of this. An increased incidence of Coulomb blockade for polycrystalline devices could reflect the presence of grain boundaries as a further source of potential fluctuations and an additional cause of tunnel barrier formation. Overall, the device characteristics were similar to those seen in lateral nanowires, both for the polycrystalline[11,12] and the single-crystal[13] devices. In accordance with these studies it seems likely that the main causes of tunnel barrier formation are potential fluctuations due to the random placement of dopant atoms and potential barriers due to grain boundaries.

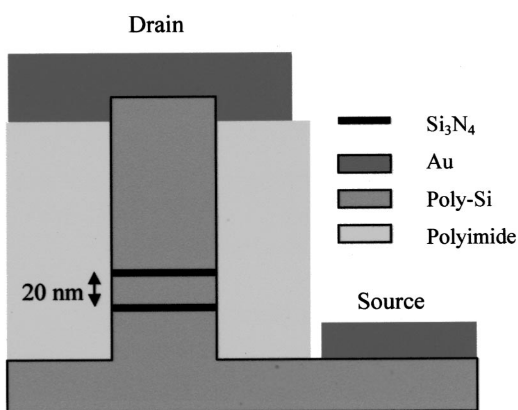

FIG. 2. Schematic of the device structure. The number of barriers is changed between zero and two.

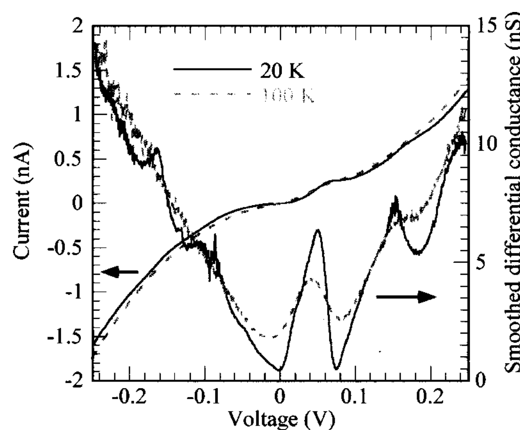

FIG. 3. $I-V$ and differential conductance characteristics of a 150 nm diam, single-barrier device at 20 K.

B. Devices with a single nitride barrier

Most devices with a single silicon nitride barrier also did not show a zero current region at 20 K but some other interesting nonlinearities were often observed in the $I-V$ curves. Figure 3 shows the $I-V$ and differential conductance characteristics of a single-barrier device with a diameter of 150 nm. Clear steps can be seen in the $I-V$ curves, which persist to over 100 K. Such steps were observed in several devices. Statistical analysis of many devices has shown that the steps do not occur at characteristic voltages and that devices with very large cross-sectional areas do not show these features. By comparison with devices without any silicon nitride layers, it was clear that the resistance of the silicon nitride barrier was much greater than any other resistance in the system. Therefore, such prominent current steps must be caused by something related to the tunneling through the nitride layer. The cause of these current steps remains uncertain at present but it is possible that they are the result of trap-assisted tunneling through trap states in the nitride or at the silicon–silicon nitride interface. The overall current densities through the nanopillars were quite low and, for future work, thinner silicon nitride layers would be preferable to increase the currents through the nanopillars and to be able to observe clearer Coulomb charging effects in devices with two or more barriers.

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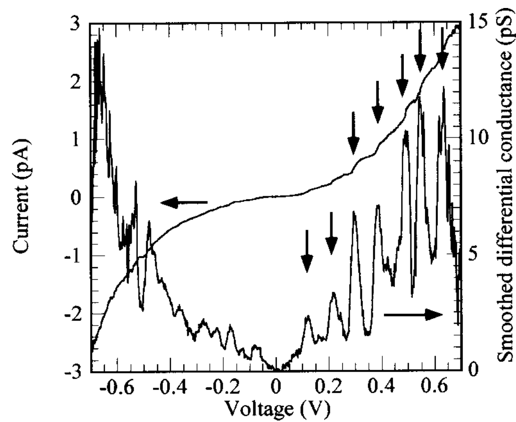

FIG. 4. $I-V$ and differential conductance characteristics of a 60 nm diam, double-barrier device at 20 K showing a Coulomb gap and staircase.

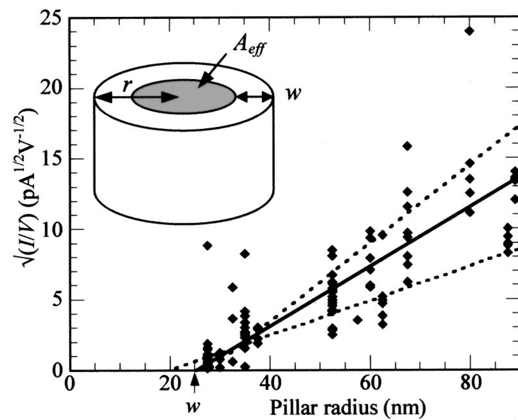

FIG. 6. Plot of the square root of conductivity vs the pillar radius at 300 K. This is used to determine the depletion width, w.

C. Devices with two nitride barriers

Figure 4 shows a $I-V$ characteristic of a 60 nm diam two-barrier device at 20 K. A zero current region and periodic current steps can be seen. The current steps are approximately 90 mV apart, similar to the size of the zero current region. These features are consistent with a Coulomb blockade explanation for charge transport. Single-electron tunneling simulations were performed in which the silicon nitride layers were treated as parallel plate capacitors and tunnel resistances were calculated based on a direct tunneling mechanism. These were found to be in reasonable agreement with the staircase characteristics which were observed. Further evidence that these effects are due to Coulomb blockade is published elsewhere.[7] Devices with diameters of 75 nm or less usually showed zero current regions at 20 K, with smaller devices generally showing larger gaps.

There was significant variation in the behavior of devices of similar dimensions and Fig. 5 shows a $I-V$ characteristic of a similar device at various temperatures. In this case, the size of the zero current region is much larger and a negative differential conductance (NDC) peak can be seen at -0.6 V. The current in this device can be seen to vary greatly as the temperature is altered. The zero current regions in all devices were shown to be thermally removed, the thermal energy required depending on the gap size. This, along with the relative rarity of Coulomb blockade in devices with fewer than two nitride barriers, rules out a multiple tunnel junction explanation for the wider gaps. This wide-gap behavior was not observed for devices with fewer than two nitride barriers.

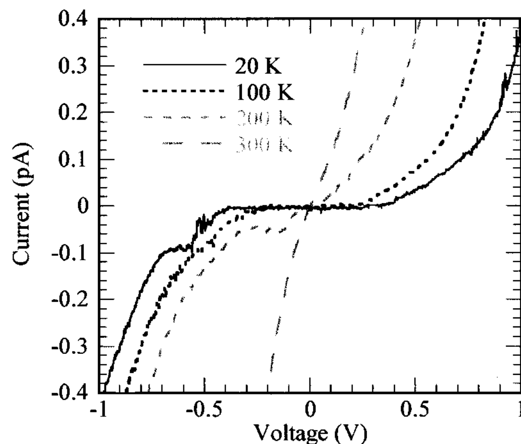

FIG. 5. $I-V$ characteristics at various temperatures for a 60 nm diam, double-barrier device showing a wide zero current region.

In order to study the conduction mechanisms, departure from the orthodox theory of Coulomb blockade due to the semiconductor nature of the pillars must be considered and the extent of carrier depletion in the pillars is a key parameter in this. Figure 6 shows a plot of the square root of the pillar conductance (at low bias) versus the pillar radius, r, for many devices. This can be used to determine a depletion width, w, and hence an effective area, A_{eff}, for the devices (see the inset in Fig. 6). The data points for different devices give a straight line (with some variation) and the intercept gives the depletion width. The depletion width was found to be 25 ± 5 nm at 300 K and 35 ± 10 nm at 20 K. A depletion width of 35 nm implies that pillars with diameters of 75 nm have, on average, only one active dopant atom within a quantum dot. Hence the smallest pillars (radius of 25–30 nm) are highly depleted at 20 K.

By treating the silicon nitride as a parallel plate capacitor we can estimate the charging energy of the island and hence the size of the Coulomb gap according to the orthodox blockade theory. For a given depletion width, we can compare the measured gap sizes with theory. Figure 7 shows a plot of the size of the zero current region versus the theoretical gap size for a depletion width of 25 nm. Note that this simple model is limited because $w>r$ cannot be used. The device with the staircase shown in Fig. 4 is in reasonable agreement with orthodox theory but most of the devices have a larger gap than the orthodox model predicts.

The absence of high-temperature zero current regions in the devices with fewer than two nitride barriers implies that the wide gaps are related to the double nitride barrier structure. The conduction through the smallest pillars is likely to involve only one or two crystallites between the two nitride barriers, the conduction bands of which could be shifted upwards by external potentials of grain boundaries and sidewalls.

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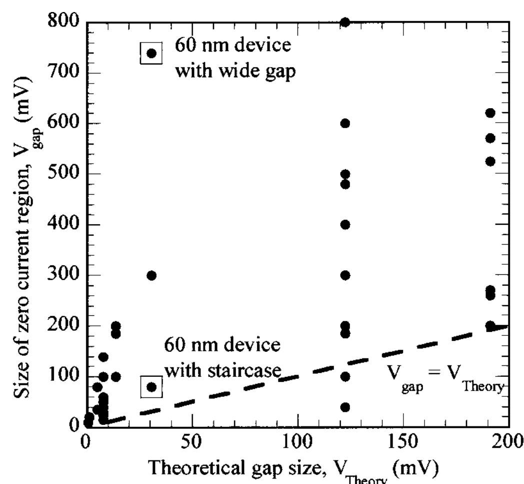

FIG. 7. Comparison of the sizes of the zero current regions with the theoretical Coulomb gap size for a depletion width of 25 nm. Most of the devices have a larger gap size than the orthodox model predicts.

Devices were also fabricated where the separation between the two silicon nitride layers was 10 rather than 20 nm. These devices tended to show larger gaps than comparable devices with a 20 nm barrier separation and often showed a prominent current step similar to the NDC in Fig. 5. These NDC features could be due to resonant tunneling but further measurements are needed to confirm this. Devices with oxidized sidewalls showed similar characteristics to the unoxidized devices for all the different layer structures, although the device yields were too low to fabricate enough devices for quantitative comparison.

We attribute the large zero current regions to the quantum dots being fully depleted due to the small number of dopant atoms and strong confinement potentials. There could be two effects contributing to this. First, the conduction band of the quantum dot could be raised by the electrostatic potentials described earlier. The conduction band offset of the quantum dot is added to the Coulomb gap size. The other is that a space charge region may form outside the nitride barriers in which a voltage drop occurs, thereby increasing the size of the Coulomb gap.[14,15] In similar studies of III–V semiconductors, a material with a lower conduction band was used in the quantum well in order to avoid the quantum dot being fully depleted at zero gate bias.[16] Nishiguchi and Oda[17] found that, in silicon structures with silicon dioxide tunnel barriers and a single undoped silicon crystallite, a high gate voltage was required before gate oscillations were observed, indicating that the conduction band of the quantum dot must be lowered before any electrons can be added. Although the quantum size effect was more likely to be important in their work, in our devices the conduction band of a single grain could easily be shifted by external potentials to enhance the size of the Coulomb gap.

In devices without nitride barriers, the tunnel barriers are much lower and may vary with applied bias, making a large, well-defined gap unlikely.

IV. CONCLUSIONS

The nanopillars without nitride layers were seen to show Coulomb blockade at low temperatures. This was common for devices of 50 nm diameter but rare for devices over 65 nm in diameter at 20 K. This behavior is similar to that observed in lateral nanowire devices. The presence of Coulomb blockade is due to a combination of factors. First, the lateral confinement due to the surface potential makes the channel width very narrow. Then, the channel is entirely pinched off in places by nonuniformities in the pillar, leading to the formation of tunnel barriers. The different types of nonuniformity that are likely to be contributing factors are potentials due to random placement of dopant atoms, defects in the crystal structure caused by reactive ion etching, and nonuniformities in the surface potential from surface roughness. Additional confinement due to grain boundaries will be present for the polycrystalline nanopillars and this explains why Coulomb blockade was occasionally seen in larger diameter polycrystalline nanopillars as well.

The single-barrier devices were useful to investigate the conduction of a small area of a single nitride barrier, so the results from devices with multiple barriers were easier to interpret. Current steps were seen in the $I-V$ characteristics of many of the single-barrier devices. The most likely explanation of this is that the direct tunneling process, which limits the current, is aided by another mechanism. Trap-assisted tunneling, through trap states in the nitride layer or at the silicon/silicon nitride interface, is a possible cause of this. The same mechanism manifests itself as randomly placed steps in the current–voltage characteristics in devices with more than one barrier.

Devices with two silicon nitride layers and diameters less than 75 nm showed zero current regions at 20 K much more consistently than zero barrier devices of similar dimensions. This is thought to be because of the two silicon nitride tunnel barriers, which are always present since they do not rely on random effects and are effective up to room temperature due to the higher barrier height. Coulomb staircases were observed for some devices, which fitted with simple estimations of tunnel barrier capacitance and resistance and single electron tunneling simulations. Wide zero current regions were also seen for some devices with sizes up to 800 mV. The wider zero current regions are attributed to fully depleted quantum dots where the raised conduction band of the quantum dot adds additional voltage to the Coulomb gap.

Oxidized devices were seen to have similar characteristics to their unoxidized relatives for all of the different layer structures but problems of low yield for the top contact prevented quantitative comparisons.

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[1] Phys. World **13**, 12 (2000); also at http://www.bell-labs.com/news/1999/november/15/vertical.pdf.

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