

# Nanoscale Coulomb blockade memory and logic devices

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## Abstract

This paper gives a brief review of our recent work done in the area of nanometre-scale Coulomb blockade (CB) memory and logic devices, that enable us to realize future electron-number scalability by overcoming inherent problems to conventional semiconductor devices. We introduce multiple-tunnel junctions (MTJs), naturally formed in heavily doped semiconductor nanowires, as a key building block for our CB devices. For memory applications, the hybrid MTJ/MOS cell architecture is described, and its high-speed RAM operation is investigated. For logic applications the binary decision diagram logic is discussed as a suitable architecture for low-gain MTJ transistors.

## 1. Introduction

Over the last few decades, performance of VLSI circuits has been steadily improved by scaling down device dimensions. In dynamic random access memories (DRAMs), for instance, the amount of charge stored per memory cell has been decreased with reduction of the cell area. After the 1 Mbit generation, however, it has become increasingly difficult to keep up such a constant decrease in the stored charge per bit because the signal becomes less immune to leakage current, internal noise, and soft errors. In microprocessors, for another example, power consumption per one MOS transistor has also been reduced due both to miniaturization and to improved operation methods. Nevertheless, the total power consumption per microprocessor has gradually been increasing along with the increase in the number of MOS transistors per chip, and the number of electrons used to switch one MOS transistor on and off needs to be further reduced to counter this trend. However, when the number of electrons becomes less than 1000, inherent charge fluctuations cause unacceptable statistical variations in the subthreshold characteristics of the MOS transistors. For both memory and logic applications, how to guarantee a future ‘scalability’ of the devices is a key issue, along with a reduction of the number of electrons. Single- and few-electron devices are expected to overcome these issues by introducing the Coulomb blockade (CB) effect [1, 2] as the new principle

for the controlled transfer of a small number of electrons. This paper reviews our recent progress of research on nanoscale devices based on the CB effects, particularly for high-speed memory and logic applications.

## 2. Heavily doped nanowires and multiple-tunnel junctions

A key building block for our nanometer-scale CB devices is the gated multiple-tunnel junction (MTJ) structure (figure 1(a)). From a device engineering point of view the MTJ structure is more suitable than a simple double-tunnel junction since it reduces co-tunnelling which generally leads to unfavourable leakage current. The MTJ structure is also robust against offset charge effects [3, 4]<sup>3</sup> which vary the Coulomb gap and may even break the CB. In our work the MTJ is realized using gated heavily doped silicon or GaAs nanowires with a few tens of nanometers in width. Although the nanowires are formed to be geometrically uniform, the electron distribution in the nanowires is not uniform because of randomly distributed dopant atoms and fluctuations in surface potentials, and isolated electron islands are naturally formed when the overall electron concentration becomes low under a negative gate bias. The nanowires can be formed either

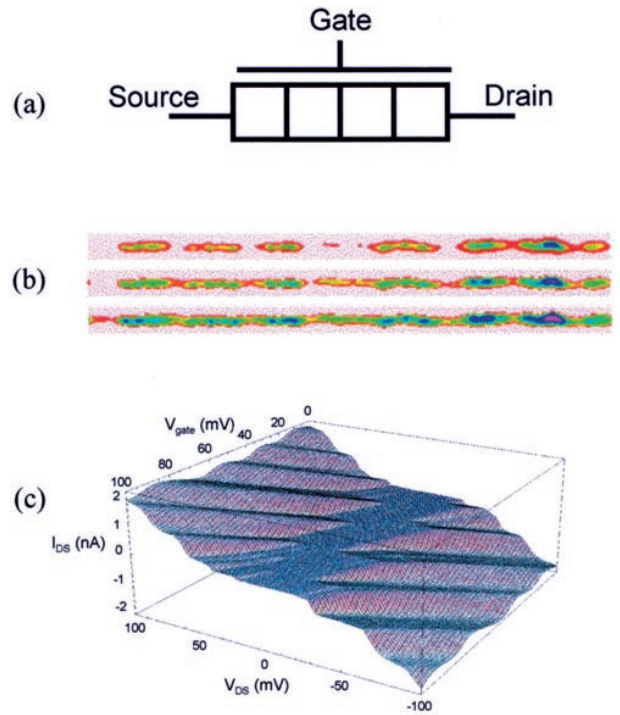
<sup>3</sup> This work was performed within the EU ESPRIT MEL-ARI project FASEM (Fabrication and Architecture of Single-Electron Memories).

vertically [5] or laterally [6], but the lateral structures have been used more often because of the simplicity in device fabrication. For the lateral nanowires the CB oscillation has been observed experimentally at a temperature of up to around 60 K, and it has successfully been applied for making nanoscale memory and logic devices. The electronic states and transport properties of the nanowires has recently been analysed using a newly developed simulation in which the randomly distributed ionized dopants in the nanowire are treated explicitly, and the electron states are calculated self-consistently under the Thomas–Fermi approximation<sup>4</sup>. Figure 1(b) shows the electron distributions simulated for a 20 nm wide and 400 nm long Si nanowire with a doping concentration of  $10^{20} \text{ cm}^{-3}$  for three different gate bias. It can be seen that the electron distribution is continuous for a low negative gate bias (the bottom one), but a few electronic islands and tunnel junctions are naturally formed on increasing the negative gate bias (the middle and upper ones). The electronic structure is almost a linear chain of thin islands which can be modelled as an ideal one-dimensional MTJ. To simulate the electrical properties of the nanowires, self-capacitances and inter-island capacitances were calculated by assuming that these electron islands have sufficiently metallic-like properties. The inter-island tunnel resistances were also evaluated approximately by finding the shortest path between the electron islands. The capacitance and tunnel resistance parameters were fed into our single-electron circuit simulator to obtain the  $I$ – $V$  characteristics of a nanowire. Figure 1(c) shows the resultant  $I_{\text{ds}} - V_{\text{ds}} - V_{\text{gs}}$  characteristics simulated for the nanowire: the CB oscillation in the  $I_{\text{ds}} - V_{\text{gs}}$  characteristics and the Coulomb staircase in the  $I_{\text{ds}} - V_{\text{ds}}$  characteristics are clearly seen.

### 3. High-speed MTJ cell for fast RAM applications

Since single-electron memory was first reported in 1993 [7], a variety of single- (or few-) electron memory structures have been reported. These single-electron memories may be classified into two groups: one is the quantum-dot (QD) cell for non-volatile memory applications and the other is the MTJ cell for fast RAM applications. In the QD cell structures, extremely small single- or multiple-QDs with diameters ranging from 1 to 10 nm are used as a floating gate. Since the electrons are confined on the memory node with a solid potential barrier due to the conduction-band discontinuity as in the FLASH memory, a long data retention time can be achieved while the write/erase times are generally rather long, typically from 1  $\mu\text{s}$  to 1 ms. The first QD cell was fabricated utilizing polycrystalline silicon (poly-Si) grains with a typical size of 3 nm naturally formed in a poly-Si quantum wire [8]. In this structure a grain acts as a floating gate of the memory cell, and the charge stored in the grain is sensed as a change in conductance between the source and drain. One problem with this structure, namely a large spread of the threshold-voltage shift, has been overcome by adopting a verify process [9], and room-temperature operation of a prototype 128 Mb memory cell array has recently been demonstrated [10]. There have also been alternative approaches to achieving the QD cells:

<sup>4</sup> Details of the simulation will be published elsewhere. This work was carried out under the management of JST/CREST.

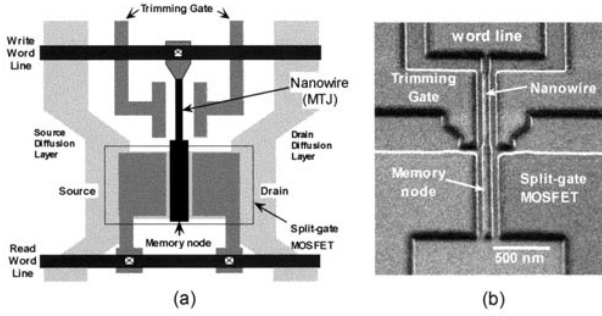


**Figure 1.** (a) A schematic symbol of a gated MTJ. (b) Electron distributions in a heavily doped ( $N_D = 1 \times 10^{20} \text{ cm}^{-3}$ ) silicon nanowire 400 nm in length and 20 nm in width simulated for three different gate bias voltages. (c) Drain current  $I_{\text{ds}}$  as a function of the source-to-drain voltage  $V_{\text{ds}}$  and the source-to-gate voltage  $V_{\text{gs}}$  simulated for the heavily doped silicon nanowire.

(This figure is in colour only in the electronic version, see [www.iop.org](http://www.iop.org))

silicon or germanium nanocrystals formed in an oxide layer by ion implantation [11] and a single nanometer-scale dot formed using a cutting edge technology [12] were successfully used as a memory node of the QD cell.

On the other hand, the MTJ cell has been designed to achieve a high-speed write operation, although its data retention time is much shorter than that for the QD cells. The MTJ cells were demonstrated first using a side-gated  $\delta$ -doped GaAs nanowire [7] and also by using a heavily doped Si nanowire formed on an SOI substrate [13]. An advanced MTJ cell structure, L-SEM (lateral single-electron memory), has also been proposed [14–17] so as to achieve compatibility between the MTJ transistors and peripheral CMOS sense circuits. In the L-SEM cell, the MTJ formed using a heavily doped Si nanowire with a width of about 50 nm is integrated into the nanoscale memory node on a split-gate MOSFET. Figures 2(a) and (b) show the schematic L-SEM single-cell structure and scanning electron micrograph of a fabricated L-SEM cell in which the size of the memory node is designed to be  $70 \text{ nm} \times 1 \mu\text{m}$ . For making the cell array the electrodes of the L-SEM cell are connected to the source and data lines and read and write word lines (see figure 2(a)). In the write operation electrons tunnel through the MTJ onto the memory node by applying the write word line (WWL) voltage  $V_{\text{WWL}}$ . Stored memory node voltage  $V_{\text{node}}$  is read through the current in a split-gate MOSFET (see figures 2(a) and (b)), and the L-SEM cell, therefore, has gain and a large  $S/N$  ratio. The two gates besides the central memory node act as switch transistors



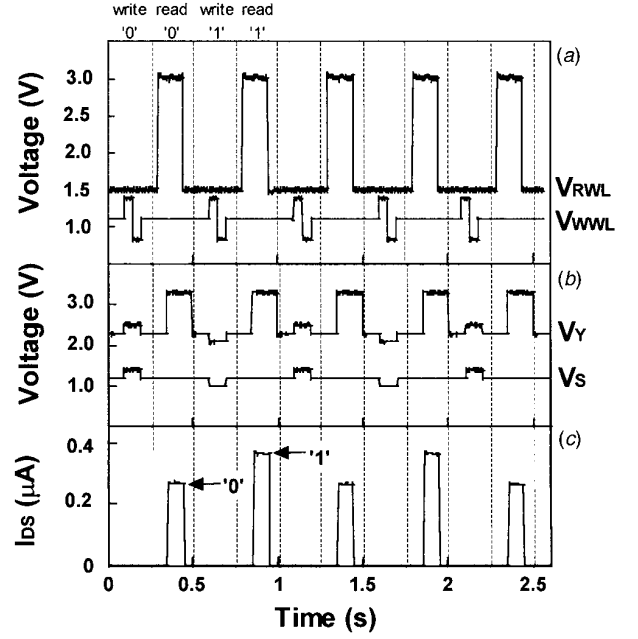
**Figure 2.** (a) An in-plane L-SEM cell layout with a split-gate sense MOS transistor and (b) a perspective SEM micrograph of a fabricated L-SEM cell.

to connect the memory node to the data line. This sense transistor structure enables us to select a particular row of the memory array by applying a read word line (RWL) voltage  $V_{RWL}$  without disturbing the stored data. In the optimized structure, it has been shown that a change in the memory node voltage from  $-50$  mV ('0' state) to  $50$  mV ('1' state) leads to an increase in  $I_{ds}$  from  $1$  nA  $\mu\text{m}^{-1}$  to  $1$   $\mu\text{A}$   $\mu\text{m}^{-1}$  [15, 16], which is large enough to be detected by standard sense amplifiers.

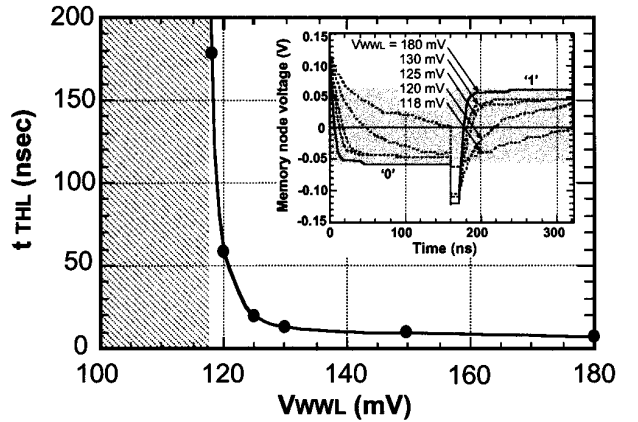
High-speed read/write operation of the L-SEM has been demonstrated theoretically and experimentally [14–19]. Figure 3 shows the experimental read/write waveforms observed for the  $3 \times 3$  L-SEM cell array [19]. Figure 3(a) and (b) are the cycle timing diagrams for the WWL/RWL and the source/data lines, respectively. To write '0' ('1') to the L-SEM cell, a common positive (negative) bias voltage  $V_{sy}(=V_s=V_d)$  is applied both to the source and data lines, and a cyclic voltage  $V_{WWL}$  is applied to the WWL. The bottom figure shows the current through the sense MOSFET, and the '0' and '1' current levels are clearly seen. Fast switching properties of the L-SEM have been investigated by performing transient simulation. In the inset to figure 4, the time-dependence of the memory node voltage  $V_{node}$  (solid curve) is shown for various values of  $V_{WWL}$ . The switching time  $t_{THL}$  of the L-SEM depends largely on  $V_{WWL}$ . As shown in figure 4 the switching occurs above a certain threshold voltage, and  $t_{THL}$  can be decreased to less than  $10$  ns by choosing an appropriate value of  $V_{WWL}$ , which is comparable to that of conventional DRAMs. This is simply because a larger tunnelling current flows through the MTJ on increasing  $V_{WWL}$ , and the switching time approaches the limit determined by  $C_{\Sigma} \cdot R_t$  where  $C_{\Sigma}$  and  $R_t$  are the total memory node capacitance and MTJ tunnel resistance. The fast writing operation of the L-SEM has also been verified experimentally by applying a short writing pulse down to  $10$  ns [18].

#### 4. CB binary decision diagram logic device

In logic applications the MTJ transistor is again a key element with the advantage of low power consumption owing to a small number of electrons in the transistor operation [20–22]. On the other hand, the MTJ transistor has the disadvantage of low gain, and we cannot simply apply standard CMOS logic architecture for the CB logic circuits. To overcome this issue, we employed 'binary decision diagram (BDD) logic' architecture [23], which is analogous to MOS pass-transistor logic. Figure 5(a) shows a BDD AND logic circuit formed with eight

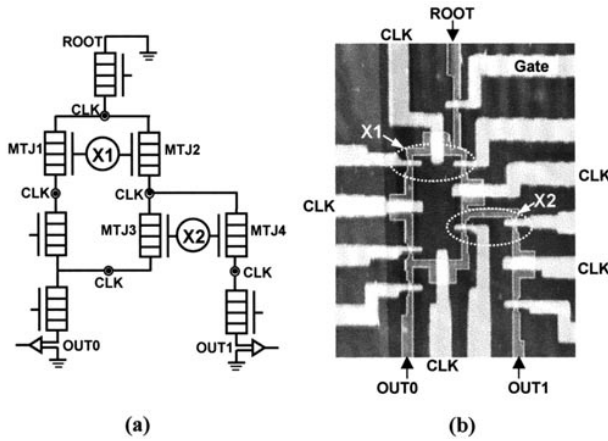


**Figure 3.** Experimental read/write waveforms measured for a  $3 \times 3$  L-SEM cell array at  $20$  K. Taken from [19].

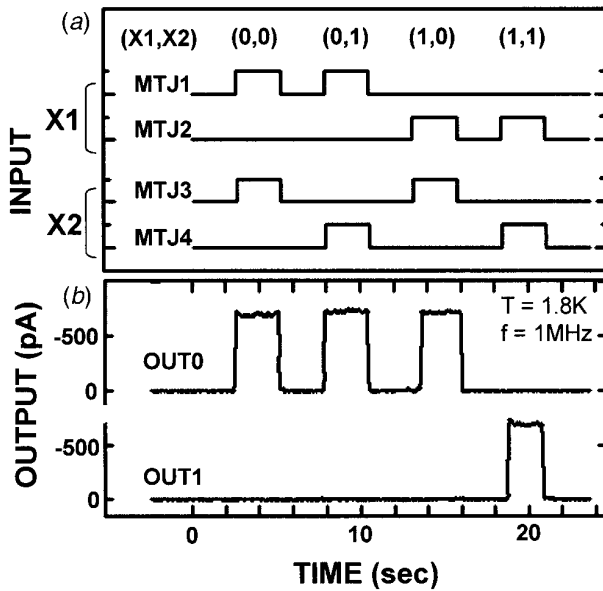


**Figure 4.** Switching time  $t_{THL}$  as a function of  $V_{WWL}$ , simulated for the L-SEM at  $4.2$  K. The hatched region indicates the voltage region in which no switching is observed. The inset shows transient memory node voltage in the write operation was simulated for various values of  $V_{WWL}$ . The grey area represents the CB gap of the MTJ of the silicon nanowire.

MTJ transistors [24]. This BDD circuit consists of the root, two decision-making nodes  $X1$  and  $X2$ , and two output leaves  $OUT0$  and  $OUT1$ . At each node we adopt a two-way switch to direct electrons to the left or the right, which does not need a large gain but only a good ON/OFF switching characteristic. In our BDD device the two-way switch is made using two MTJ transistors [25] as shown in figure 5(a). At the  $X1$  node the electron packet takes the left-hand path when the left MTJ transistor (MTJ1) is at the ON state and the right hand one (MTJ2) is at the OFF state. This configuration represents an input  $X1$  of '0'. The other configuration in which MTJ1 is OFF and MTJ2 is ON represents an input  $X1$  of '1'. Figure 5(b) shows an AFM image of the AND device composed of GaAs-based MTJ transistors. Two decision-making nodes are shown by the dotted circles with  $X1$  and  $X2$ .



**Figure 5.** (a) An equivalent circuit of the CB BDD AND function circuit and (b) an AFM image of the fabricated AND circuit based on eight GaAs MTJ transistors. Taken from [24].



**Figure 6.** Input signal timing diagram for X1 and X2 (a) and output signal currents at OUT0 and OUT1 measured at 1.8 K with  $V_p = 100$  mV (b). Taken from [24].

The CB BDD device is operated in the pumped mode by applying phase-controlled triangular-shaped clocking pulses to the clocking gates CLK. Since the clocking voltage  $V_p$  is chosen to be a little above the CB gap of the MTJs and the voltage supply  $V_{DD}$  is kept at zero, a small number of electrons flow only for a short period of time, transferring an electron packet from one node to the next. However, it has been demonstrated very recently by simulation that such a pump operation often causes an unfavourable reverse flow of electrons. These electrons do not contribute to the net current of the circuit, but increase power consumption in the circuit. To avoid the reverse electron flow the gate bias voltages applied to each MTJ transistors, especially those for the first and last ones, should be chosen carefully. The optimal operation conditions for zero reverse flow, i.e. minimum power consumption, can theoretically be found using multiple stability diagrams [26].

Figure 6 shows an experimental input–output waveform obtained for the AND device at 1.8 K with a clocking frequency  $f$  of 1 MHz and  $V_p$  of 100 mV [24]. Figure 6(a) shows the input signals (X1, X2), and figure 6(b) the output signals OUT0 and OUT1 which clearly represent the results  $\bar{X}_1 \cdot \bar{X}_2$  and  $X_1 \cdot X_2$ , respectively. The amplitude of the output signals decreases linearly as  $V_p$  decreases since a number of electrons carried in a packet is reduced. For our AND device the minimum possible  $V_p$  was found to be about 25 mV, and the output waveforms are largely distorted for  $V_p$  values below that. The number of electrons per packet  $n$  can be estimated from the clocking frequency dependence of the output current using the simple formulation,  $I = n \cdot e \cdot f$  where  $e$  is the elementary charge. It was observed that the output current increases at frequencies up to 1 MHz, and deviates from the linear relationship as the RC time delay of the MTJs is pronounced at higher frequencies. From the observed linear dependence region, it was found that  $n = 1080$  for  $V_p = 100$  mV and can be reduced to 160 for  $V_p = 25$  mV, which is the smallest number of electrons per cycle in the present BDD AND device.

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