

Carrier Transport across a Few Grain Boundaries in Highly Doped Polycrystalline Silicon

Yoshikazu FURUTA^{1,4,*}, Hiroshi MIZUTA^{1,4}, Kazuo NAKAZATO^{1,4}, Yong T. TAN^{2,4}, Toshio KAMIYA^{2,4}, Zahid A. K. DURRANI^{2,4}, Haroon AHMED^{2,4} and Kenji TANIGUCHI³

¹Hitachi Cambridge Laboratory, Madingley Road, Cambridge CB3 0HE, U. K.

²Microelectronics Research Centre, Cavendish Laboratory, University of Cambridge, Madingley Road, Cambridge CB3 0HE, U. K.

³Electronics, Information Systems and Energy Engineering, Osaka University, 2-1 Yamada-oka, Suita, Osaka 565-0871, Japan

⁴CREST JST (Japan Science and Technology), Shibuya TK Bldg., 3-13-11 Shibuya, Shibuya-ku, Tokyo 150-0002, Japan

(Received January 15, 2001; accepted for publication April 16, 2001)

We have fabricated nanometer-scale point-contact devices in 50-nm-thick poly-Si films with a grain size of from 150 nm to 20 nm. Both linear and nonlinear I_{ds} - V_{ds} characteristics were observed in these devices, corresponding to a channel without a grain boundary (GB) and that with a single or a few GBs, respectively. The temperature dependence of resistivity indicated that the effective potential barrier height qV_B of the GBs for the devices which show the nonlinear I_{ds} - V_{ds} characteristics ranges from 30 meV to 80 meV. We discussed percolation conduction of electrons through a few GBs due to nonuniform GB properties in heavily doped poly-Si films.

KEYWORDS: polycrystalline silicon, electron transport, grain boundary, point-contact device, potential barrier height, intergrain

Polycrystalline silicon (poly-Si) has been widely studied for various applications such as thin film transistors, static random access memories (SRAMs) and stacked memory cells.^{1,2)} The electrical properties of poly-Si films are sensitive to the process conditions, particularly those of crystallization and passivation methods. Significant efforts have been made to increase the carrier mobility of these films since this limits the ON current of poly-Si devices. Thin poly-Si films have also been studied as a building block for single-electron memories^{3,4)} where individual silicon grains are used as charging islands. In this application, poly-Si films with a grain size of less than 10 nm are used, such that the single-electron charging energy is sufficiently large to observe Coulomb blockade effects.

Despite these intensive studies, the relationship between the microscopic properties of an individual grain boundary (GB) and the macroscopic electric properties of poly-Si films is not clear. Very recently, a detailed investigation has been reported for 1- μ m-thick poly-Si films with a grain size of about 0.3 μ m.⁵⁾ In this study, electron transport through a small number of GBs has been measured for the first time by using a four-point probe technique, and the distribution of individual GB potential barrier height has been investigated. It has been shown that for low-doped devices with a donor concentration of $1 \times 10^{17} \text{ cm}^{-3}$, the GB potential barrier height varies largely among devices, and this has been attributed to nonuniformity of potential barrier heights of GBs.

In this paper, we focus on the relationship between the local structure and transport properties of heavily-doped poly-Si films with a much smaller film thickness and grain size. By fabricating novel ultrashort point-contact devices where both the length and width of the channel are as small as the grain size, we study electron transport through a single or a few GBs in the channel. The main objectives of this study are to investigate the transport properties of a single GB and to establish “GB engineering” techniques.

Highly doped poly-Si films were prepared as follows: A 40-nm-thick SiO_2 layer was thermally grown on a (100)-oriented lightly-doped silicon substrate. An undoped 50-nm-

thick amorphous silicon (a-Si) film was then deposited using low-pressure chemical vapor deposition (LPCVD) at 550°C, followed by phosphorus ion implantation into the a-Si film layer with an energy of 20 keV at a dose of $3 \times 10^{14} \text{ cm}^{-2}$. Solid-phase crystallization (SPC) of the a-Si films was performed at 850°C for 30 min in an Ar ambient, crystallizing the films as well as activating the dopants electrically. By using a simulator ATHENA,⁶⁾ the doping concentration in the poly-Si film was estimated to be as high as 10^{20} cm^{-3} .

Side-gated point-contact device structures (see Fig. 1(a)) were defined by using a conventional electron-beam lithography technique with polymethylmethacrylate (PMMA) resist. The devices were electrically isolated by reactive ion etching into the silicon substrate with a mixture of SiCl_4 and CF_4 . Figure 1(b) shows a scanning electron microscope (SEM) image of a Secco-etched⁷⁾ SPC thin poly-Si film. The grain size of the films after SPC ranges from 20 nm to 150 nm, which is consistent with the cross-sectional transmission electron microscope (XTEM) observation. The XTEM observation

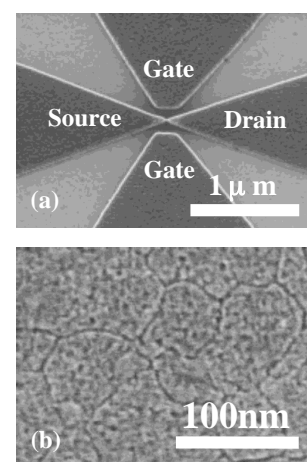


Fig. 1. (a) Scanning electron micrograph of a point-contact device with a channel length of about 40 nm and a channel width of about 40 nm after device isolation. (b) An SEM image of a poly-Si film after Secco etching. GBs are clearly delineated. The size of grains ranges from 20 nm to 150 nm.

*E-mail address: furuta@phy.cam.ac.uk

shows that the geometry of the grains is columnar and perpendicular to the surface. Since the channel dimensions (width and length) of the point-contact devices were in the range of 30 nm–50 nm, the channel may contain no GB or a few GBs at most.

Source-to-drain current–voltage (I_{ds} - V_{ds}) characteristics were measured for more than 30 devices at from room temperature down to 19 K. These characteristics are of two types, and typical characteristics of each type are shown in Figs. 2(a) and 2(b). Linear and nonlinear I_{ds} - V_{ds} characteristics were obtained for Device A and Device B with the same channel length of 50 nm and width of 40 nm. The resistivity for Device B at $V_{ds} \approx 0$ in Fig. 2(b) is determined to be approximately five times larger than that for Device A (see Figs. 2(c) and 2(d)). Nonlinear I_{ds} - V_{ds} characteristics were observed in about one-third of the fabricated devices, and the other devices showed linear characteristics. Moreover, a slight asymmetry in the I_{ds} - V_{ds} characteristics was observed among devices with nonlinear characteristics. It should be noted that no Coulomb blockade oscillation was observed by sweeping a side-gate bias; thus, nonlinear I_{ds} - V_{ds} characteristics are attributed to the GB potential barrier of GBs in the channel.

We analyzed the temperature dependence of the resistivity at above 200 K to obtain the local potential barrier height qV_B of a GB. Assuming a thermionic emission current via GBs, the current density J is given by^{8,9)}

$$J = qnv_c \exp\left(-\frac{qV_B}{k_B T}\right) \sinh\left(\frac{qV_{ds}}{2k_B T N}\right), \quad (1)$$

where q is the elementary charge, v_c the collection velocity of electrons, T the film temperature, n the carrier concentration and N the number of GBs between contacts. By fitting eq. (1) to the experimental I_{ds} - V_{ds} curve, the value of N can be obtained. The value of $N \approx 3.5$ was obtained for one of the largest devices with a channel length of 50 nm and width of 50 nm. N is also found to be virtually temperature independent above 200 K. It is very likely that the number of GBs in the channel is less than four in all devices. Since the I_{ds} - V_{ds} characteristics of the devices are determined by the electric properties of the narrow channel region, qV_B can be evaluated from the measured temperature dependence of the resistivity (see Figs. 2(c) and 2(d)) using eq. (1). The

distribution of qV_B for devices with nonlinear I_{ds} - V_{ds} characteristics is shown in Fig. 3 and that for devices with linear I_{ds} - V_{ds} characteristics is shown in the inset of Fig. 3. Note that the devices with nonlinear I_{ds} - V_{ds} characteristics show a wide range of barrier heights from 30 meV to 80 meV, but the devices with linear I_{ds} - V_{ds} characteristics show a very sharp distribution with a mean value of approximately 30 meV. The small variation of qV_B for the devices with linear I_{ds} - V_{ds} characteristics is attributed to the average potential barrier height of many GBs in the large source and drain regions outside the channel. On the other hand, the distribution of qV_B for the devices with nonlinear I_{ds} - V_{ds} characteristics represents the GB potential barrier height in the channel. It was observed that for devices with nonlinear I_{ds} - V_{ds} characteristics, qV_B decreases with channel width and increases with channel length. In the devices with linear I_{ds} - V_{ds} characteristics, qV_B has no dependence on either channel length or width. This also suggests that the electron transport can be described as percolation conduction through local potential minima of GBs: qV_B can be different among adjacent GBs, and electrons can choose the GB with the lowest qV_B as an energetically favourable path. Therefore, when the channel width is increased, a GB with lower qV_B may exist in the channel. The increase in qV_B with the channel length is simply explained by the existence of multiple GBs including those with higher qV_B along the conduction path.

There are two possible causes of the variation of the potential barrier height of the GBs. One is the nonuniform intergrain distance between two adjacent grains. From high-resolution XTEM observations, it was found that the intergrain thickness ranges up to 1.2 nm in our poly-Si films. The intergrain contains a high density of dangling bonds which create defect states near the middle of the band gap and act as trapping sites for carriers. Therefore, more trapped carriers are expected near thicker intergrain regions, resulting in a higher potential barrier height. In addition, the defect density in the intergrain can be affected by the crystal orientations of the adjacent grains. Since poly-Si films may have grains with different orientations, the local defect density in the intergrain may vary depending on the orientations of the grains nearby. The other possible cause is the difference in the active dopant concentration in the adjacent grains. During

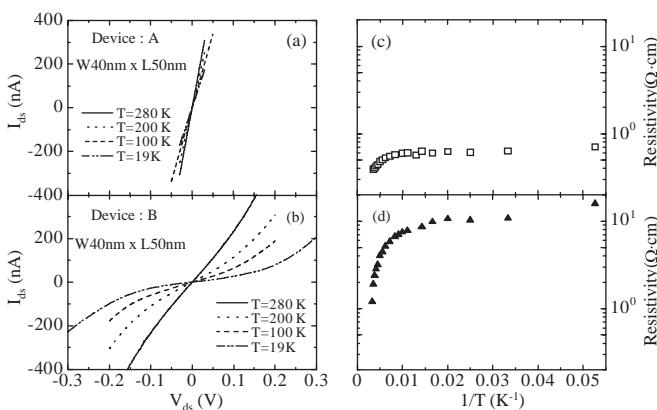


Fig. 2. (a) and (b) show source-to-drain current–voltage characteristics for Device A and Device B with a width of 40 nm and a length of 50 nm at temperatures ranging from 19 K to 280 K, respectively. (c) and (d) show the temperature dependence of resistivity of Device A and Device B.

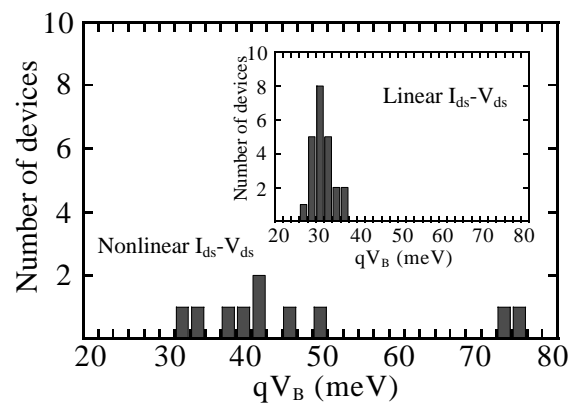


Fig. 3. Distribution of potential barrier height qV_B for the devices with nonlinear I_{ds} - V_{ds} characteristics. The inset shows that for the devices with linear I_{ds} - V_{ds} characteristics.

annealing process, some phosphorus atoms segregating into GBs become electrically inactive. The percentage of these segregated atoms relative to all the phosphorus atoms will be larger for a smaller grain. As the size of individual grains is different as shown in Fig. 1(b), the density of active phosphorus atoms in the grains may also be different depending on the grain size. These imply that the local Fermi energy relative to the conduction band edge may not be the same among the adjacent grains, also leading to a nonuniform qV_B . Finally, it should be noted that the small current asymmetry observed for the devices with nonlinear I_{ds} - V_{ds} characteristics may be attributed to unbalanced local Fermi energies among the adjacent grains.

In conclusion, the local nonuniform properties of heavily doped poly-Si films were investigated using nanometer-scale point-contact devices. It was found that for devices with nonlinear I_{ds} - V_{ds} characteristics, the effective potential barrier height qV_B of a single or few GBs ranges from about 30 meV to 80 meV. The wide range distribution of qV_B 's may result from nonuniform local defect states.

The authors would like to thank Professor S. Oda and

Mr. K. Nishiguchi of the Tokyo Institute of Technology for their continuous support and also Dr. D. Williams of the Hitachi Cambridge Laboratory for his support in SEM observations. The authors are also grateful for the many valuable discussions with Dr. T. Shimada and Dr. G. Kawachi of Hitachi Ltd.

- 1) K. Nakazato, K. Itoh, H. Mizuta and H. Ahmed: *Electron. Lett.* **35** (1999) 848.
- 2) H. J. Cho, F. Nemati, P. B. Griffin and J. D. Plummer: 1998 Symp. VLSI Technology Dig. Tech. Papers, Honolulu, 1998, p. 38.
- 3) K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai and K. Seki: *Appl. Phys. Lett.* **67** (1995) 828.
- 4) K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai and K. Seki: *IEEE Trans. Electron Devices* **41** (1994) 1628.
- 5) J. W. Tringe and J. D. Plummer: *J. Appl. Phys.* **87** (2000) 7913.
- 6) *ATHENA User's Manual* (SILVACO International, Santa Clara, CA, 1996).
- 7) F. Secco d'Aragona: *J. Electrochem. Soc.* **119** (1972) 948.
- 8) T. Kamins: *Polycrystalline Silicon for Integrated Circuits & Display* (Kluwer, Boston, 1998) 2nd ed.
- 9) J. Y. W. Seto: *J. Appl. Phys.* **46** (1975) 5247.