Analysis of multiphase clocked electron pumps consisting of single-electron transistors

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(Received 25 October 2000; accepted for publication 30 January 2001)

Pump circuits consisting of single-electron transistors are analyzed in which electrons are pumped by multiphase clock pulses. An optimal low-temperature operation condition is presented where pumped current is maximized, yet the power consumption is not. Approximate formulas for the number of electrons transferred per clock cycle and the power consumption are derived for that condition, which clearly show the advantage of the pump circuits for low-power applications. The power consumption becomes even less at higher temperatures. However, the relatively large island capacitance between transistors limits the operation temperature. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1358314]

I. INTRODUCTION

The ability to control the transfer of single electrons is a distinctive feature of single-electron devices. Some of them, including the single-electron turnstile[1] and the single-electron pump,[2] are able to transfer electrons one by one synchronized with some clock signal. There have been some proposals for circuit construction which exploit the precision control of single electrons.[3–5] In those circuits, presence or absence of a single excess electron represents a single bit.

Tsukagoshi *et al.* later experimentally demonstrated the operation of electron pump circuits composed of multiple tunnel junctions (MTJs).[6,7] The MTJs were formed in side-gated δ-doped GaAs wires.[8,9] By applying a negative voltage to a side gate, ultrasmall islands appeared in the two-dimensional electron gas (2DEG) layer due to randomly distributed dopant atoms. In addition, within a certain range of side-gate bias voltage, the side gate also worked as a single-electron transistor gate, thereby turning an MTJ into a transistor. Two types of pumps were studied by them. One consisted of a pair of MTJ transistors and was driven by an ac clock signal.[6,10] It was also referred to as the bidirectional electron pump. The other contained three or more MTJ transistors and was driven by unipolar multiphase clock pulses,[7] as shown in Fig. 1. We look into the latter multiclocked pump circuit in this article.

In spite of its apparent resemblance to the ''original'' single-electron pump,[2] the operation principle of Tsukagoshi's multiclocked pump is quite different from that of the original one. In the case of the original pump, all the capacitances contained in a device are of the same order. Consequently, it is indivisible in the sense that one has to consider the condition of Coulomb blockade taking the entire device into account. On the other hand, Tsukagoshi's pump involves two different capacitance scales. One is of the capacitances that constitute an MTJ transistor and the other is of the capacitances of clocking gates. The clocking-gate capacitances, which are situated between MTJ transistors, are considerably larger than other capacitances in the pump. As a result, component MTJ transistors work virtually independently of one another as if being voltage biased, and basically the pump operation reflects the MTJ transistors' $I-V$ characteristics rather than the precise charge configuration in the circuit. In other words, Tsukagoshi's pump is essentially a series connection of ac biased single-electron transistors.[11] It implies that the pump is not very suitable for transferring precisely one electron per cycle. If one calculates the number of electrons transferred per cycle N_c from the net current I and the clock frequency f using the relationship $I=N_c e f$, N_c is typically a few tens to several hundred. However, the pump is still a ''single-electron'' device in the sense that it utilizes Coulomb blockade of single-electron transport as will be elaborated upon later.

From a perspective of application, the multiclocked pump is potentially useful as a building block of binary decision diagram (BDD) logic circuits.[5] Some experiments have already been conducted along the lines.[12,13] However, the pump's charge transport mechanism and its possible performance have not been well-understood yet. Among other things, power dissipation is of great interest. In the conventional complementary metal–oxide–semiconductor logic circuits, the power of a logic gate is

$$P=f\times q\times V_{\mathrm{dd}}, \tag{1}$$

where $q=C_L V_{\mathrm{dd}}$ is the amount of charge that flows from the dc supply line to the ground per clock cycle, V_{dd} is the dc supply voltage, and C_L is the effective load capacitance.[14] Since the pump does not have any dc bias, the common way to estimate the power is not directly applicable. The purpose of this article is to analyze the operation of the pump circuit within the semiclassical model and to evaluate the power dissipation, with the said application in mind. The next section describes the basic theory whereby we perform analysis

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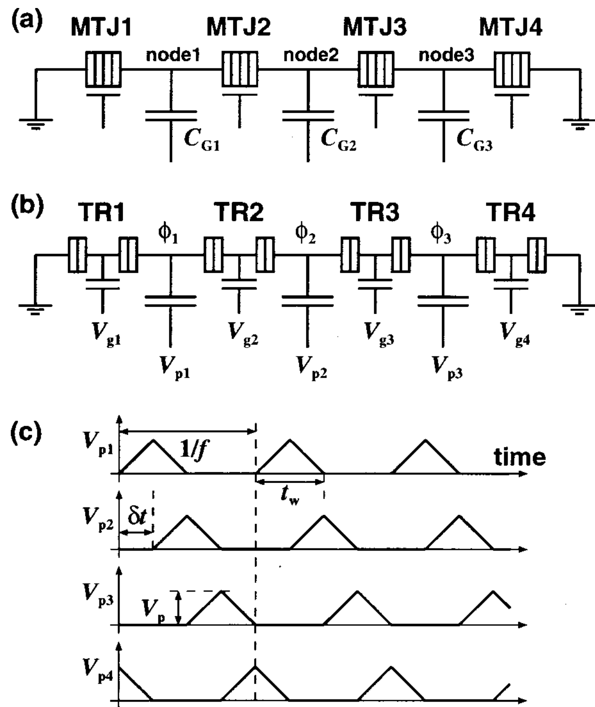

FIG. 1. The pump consists of three or more MTJ transistors and is driven by multiphase clock pulses. Electrons are pumped from the left to the right. Clocking-gate capacitances C_{Gi} are much larger than other capacitances. (a) Pump circuit with four MTJ transistors. (b) A simpler model with MTJ transistors being replaced by two-junction transistors. (c) Up to four triangular pulses are used to drive the pump. Each pulse overlaps with the pulses applied to adjacent clocked nodes. $t_w = 1/2f$ and $f\delta t = 0.25$ are taken unless otherwise specified. V_{p4} is not used in (a). It is used if a pump contains more than four MTJ transistors.

and simulations. The simplified model used in this article is presented in Sec. III. Section IV is devoted to the analysis of the pump operation at the low temperature limit. Approximate formulas for the number of electrons transferred per clock cycle and the power consumption are derived. The effect of finite temperature and the upper bound of operation frequency are treated in Sec. V. Finally, an outlook for scaling down and the logic circuit application is discussed in the last section.

II. ENERGY DISSIPATION AND TUNNELING

Semiclassical treatment of single-electron circuits with the global rule of Coulomb blockade is known to work reasonably well for application-oriented circuit analyses.[15] We apply it to pump circuits consisting of tunnel junctions, capacitors, voltage sources, and ideal leads. The amount of energy dissipation is what one needs to know to calculate tunneling rates and to evaluate the power consumption of the circuit. Let U and W_e be, respectively, the electrostatic energy and the work done by the voltage sources. The energy W_e supplied to the circuit will ultimately be transferred to the environment as heat, whatever the actual physical processes involved may be.[16] Under the global rule, the overall dissipation process is assumed to be fast enough. The electrical work performed by voltage sources is irreversible, and so is the heat transfer from the circuit to the environment. We therefore do not know the amount of entropy generated by these processes. However, by the principle of conservation of energy,

$$dU = đW_e + đQ_{\mathrm{irrev}}, \tag{2}$$

where, following the convention of thermodynamics, $đQ_{\mathrm{irrev}} = \Delta F = F(t+\Delta t) - F(t)$ is the heat added to the system within the time interval t and $t+\Delta t$. Here we have introduced an energy function

$$F = U - W_e. \tag{3}$$

Thus $-đQ_{\mathrm{irrev}} = -\Delta F$ is the energy transferred to the environment, and $-\Delta F/\Delta t$ is the power dissipation. We evaluate the energy consumption and the power using a cumulative total of ΔF for a simulation run. Evidently, it almost equals $-W_e$ over the long run.

Single-electron systems can be characterized as systems with noticeable electrostatic energy change ΔU due to transport of a single electron. Given the current–voltage function $I(V)$ of a voltage-biased tunnel junction, the rate of single-electron tunneling in the positive direction is[17]

$$\Gamma = \frac{I(-\Delta F/e)}{e} \frac{1}{1-\exp(\Delta F/k_B T)}. \tag{4}$$

Here ΔF is the change in F associated with the tunneling event and $-\Delta F/e$ is the effective bias voltage across the tunnel junction. At the limit of $\Delta U \to 0$, the evident result for a nonsingle-electron case, $\Delta F = -eV$, is naturally recovered. We use $I(V) = V/R_T$ in our simulations, where R_T is the so-called tunnel resistance. Although an Ohmic $I-V$ relation is a crude approximation, it is acceptable in this study because, in the multiclocked pump, the voltage across each transistor does not exceed the Coulomb blockade gap voltage very much.

III. MODEL

As mentioned earlier, clocking-gate capacitances C_{Gi} are assumed to be sufficiently larger than other capacitances in the circuit. It ensures that tunneling of an electron onto or out of a clocked node does not change its voltage significantly. Each MTJ transistor, therefore, may be regarded as being voltage-biased with relevant island potential(s) ϕ_i and side-gate bias V_{gi}.[10,18,19] We approximate each MTJ transistor with a two-junction single-electron transistor[20,21] as shown in Fig. 1(b). This approximation was also employed to analyze the bidirectional electron pump.[6,10] We further assume the pump to be uniform; that is, all transistors and C_{Gi} are the same. We analyze the operation of the pump circuit under these constraints.

The effective isolation of component transistors enables us to analyze the pump circuit using the Coulomb blockade stability diagrams of each individual transistor. A single-electron circuit is in a Coulomb blockaded state (or stable) if no tunneling event is energetically favorable. The stability condition for the two-junction single-electron transistor shown in Fig. 2 is derived as follows. Supposing the change in all V_j during a tunneling event is negligible, the electrostatic free energy Eq. (3) may be written as

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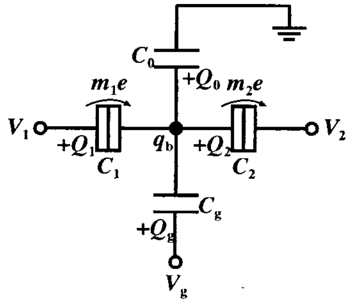

FIG. 2. Two-junction single-electron transistor. m_1 and m_2 are the numbers of charges that have tunneled through C_1 and C_2, respectively. q_b is the background charge.

$$F(m_1,m_2)=\frac{Q_1^2}{2C_1}+\frac{Q_2^2}{2C_2}+\frac{Q_g^2}{2C_g}+\frac{Q_0^2}{2C_0}-Q_gV_g$$
$$-(m_1e+Q_1)V_1-(-m_2e-Q_2)V_2, \qquad (5)$$

where m_1 and m_2 are the numbers of charges that have tunneled through junctions C_1 and C_2, respectively. By eliminating all the Q_i in Eq. (5) we obtain

$$F(m_1,m_2)=\frac{1}{2C_\Sigma}[(m_1-m_2)e+q_b+C_gV_g]^2$$
$$-\frac{m_1e}{C_\Sigma}[(C_2+C_g+C_0)V_1-C_2V_2]$$
$$-\frac{m_2e}{C_\Sigma}[C_1V_1-(C_1+C_g+C_0)V_2]$$
$$+\text{const}, \qquad (6)$$

where $C_\Sigma=C_1+C_2+C_g+C_0$ and q_b is the background charge on the central island. The constant term does not depend on m_1 nor m_2. The background charge shall be assumed to be zero from now onward. The stability condition for the neutral state $(m_1-m_2=0)$ is given by $F(\pm1,0)-F(0,0)>0$ and $F(0,\pm1)-F(0,0)>0$.[22] In the present case, the three voltage sources V_1, V_2, and V_g span a three-dimensional space. Two different cross sections of the stable region are shown in Fig. 3 as shaded areas. These diagrams shall be used extensively to analyze the pump circuit. By taking advantage of the virtual isolation of transistors, we will substitute ϕ_i and ϕ_{i+1} for V_1 and V_2 in Fig. 3 and Eq. (6). Our numerical simulation, however, does not use such an approximation method.

In the following, we mainly consider the four-transistor pump circuit shown in Fig. 1(b). The fourth clock signal V_{p4} shown in Fig. 1(c) is used only if a pump contains more than four transistors. However, it is ''reserved'' even in the case of the four-transistor pump. To put it in another way, the rising part of a pulse in V_{p1} overlaps with the tail of a pulse in V_{p4}, and not with that in V_{p3}. Although not unduly detrimental, three-clock-signal operation is prone to degrade the pump operation especially when the temperature is high, so that the use of four clock signals is preferable. The parameters used in our simulations are $C_1=C_2=2$ aF, $C_g=1$ aF, $C_0=0.5$ aF [not drawn in Fig. 1(b)], $C_G=100$ aF, and $R_T=200\,\text{k}\Omega$. With these parameters, the change in ϕ_i due to tunneling of a single electron is approximately[10] $\delta\phi\approx e/C_G\simeq1.6$ mV and sufficiently smaller than the other relevant voltage scale $e/C_\Sigma\simeq29$ mV.

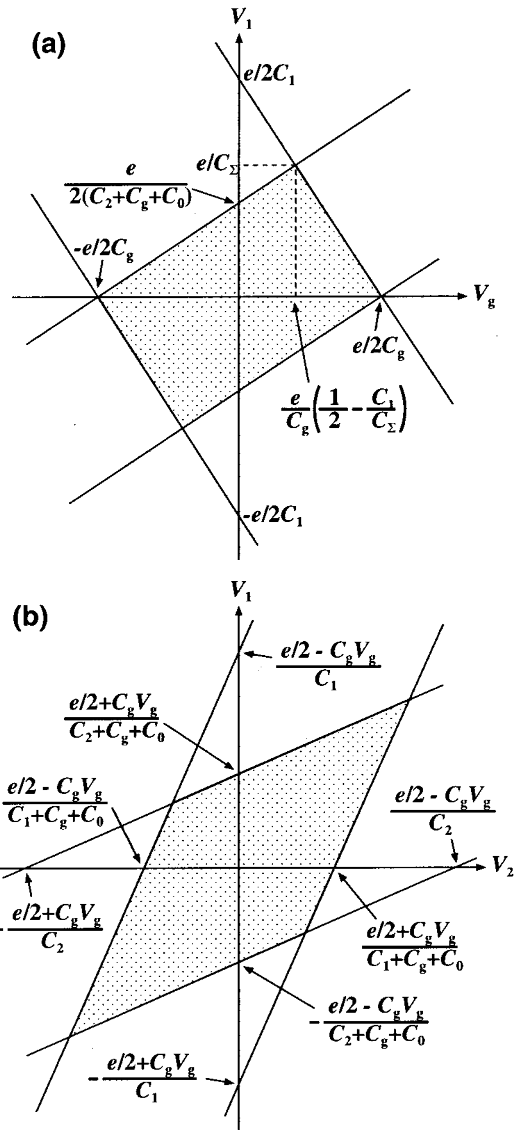

FIG. 3. Stability diagrams of the single-electron transistor. Shaded areas are the Coulomb blockade regions. q_b is assumed to be zero. (a) V_1-V_g plane at $V_2=0$, which corresponds to TR4. The cross section at $V_1=0$ (V_2-V_g plane), which corresponds to TR1, can be obtained by substituting V_2, C_1, and C_2, for V_1, C_2, and C_1, respectively. (b) V_1-V_2 plane. The rhomboid moves along the line $V_1=V_2$ if V_g is changed.

IV. CHARGE TRANSPORT AT LOW TEMPERATURE

We first focus on the electron pumping at the low temperature limit. In the case of the four-transistor pump in Fig. 1, electrons are pumped from the left end to the right end. When a clock voltage V_{pi} rises, the corresponding island voltage ϕ_i also rises and electrons flow onto the island. It should be noted that in general electrons may flow onto the island through both transistors which are connected to it. Which transistor becomes conducting depends on the potential balance in the circuit. Similarly, when V_{pi} falls, electrons may flow out of the island through both transistors. N_c is the

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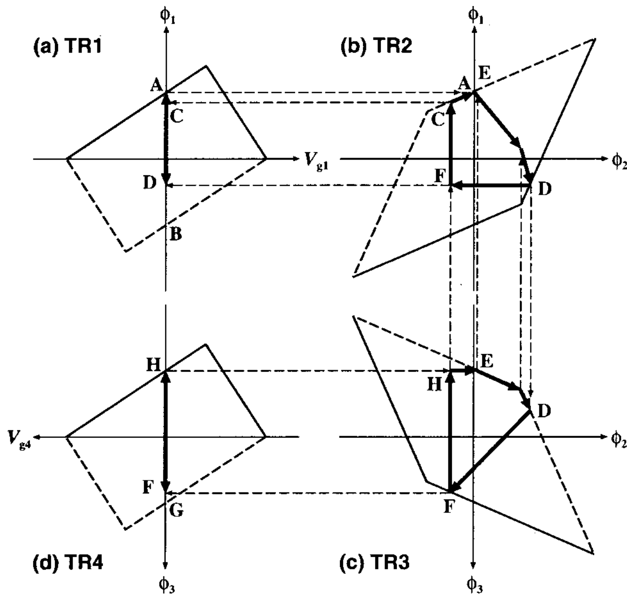

FIG. 4. A nonoptimal pump operation at $T=0$ K with all $V_{gi}=0$ V. The trajectories shown are the projection of the trajectory of the state point in a high-dimensional space onto the relevant planes. Borders for forward-direction tunneling are drawn with solid lines and those for reverse-direction tunneling are drawn with broken lines.

net number of electrons transferred per clock cycle and not necessarily the number of electrons contained in a packet that would move along the pump, if such a packet existed. Electrons that flow in the reverse direction (right to left) adversely affect the net current, that is, some electrons move back and forth within the pump without contributing to the net current while consuming energy. This can readily be confirmed by transient simulations. For the pump operation to be efficient, electrons should flow in only one direction (left to right). One way to rectify the electron flow is to make the clock pulses appropriately overlap with each other as shown in Fig. 1(c). This has empirically been known to be of crucial importance to get a net current,[7] however, it is not the sufficient condition. We will show that one may achieve almost perfect rectification by properly choosing the side-gate biases of ''edge transistors'' [TR1 and TR4 in Fig. 1(b)] while setting all other side-gate biases to zero volts.

A state of the pump can be represented by a point in the space spanned by all ϕ_i and V_{gi}. The state point moves in the space as clock pulses are applied. The pumping mechanism can be understood by considering the trajectory of the point. If the pump starts its operation from a neutral condition (without any excess charges in the pump), it settles into a steady operation mode in a few clock cycles. Figure 4 schematically shows such a steady trajectory, projected onto four planes, each of which also shows the corresponding transistor's stability rhomboid. The edge transistors are working in a somewhat different manner from other transistors, since one of their electrodes (source or drain) is grounded, so that the ϕ-V_g planes are shown for them. The $\phi_i-\phi_{i+1}$ planes are shown for other transistors.

In Fig. 4(a) the state point moves between A and D. When V_{p1} and hence ϕ_1 rises, the point moves toward A. However, before it reaches A, it reaches C in Fig. 4(b) and undesirable, reverse-direction tunneling through TR2 becomes energetically favorable. Then, provided the clock frequency f is not too high, the point moves to A along the border repeatedly crossing it owing to the competing effect of tunneling and increasing V_{p1}: tunneling lowers ϕ_1 by $\delta\phi$ per tunneling event and V_{p1} raises ϕ_1. Meanwhile, ϕ_2 becomes higher since node2 loses some electrons. Once the state point reaches A, transistor TR1 becomes conducting and the point is nearly pinned there until $V_{p1}=V_p$ because no other border is crossed anywhere else. Thus electrons enter the pump through the entrance transistor TR1 at A.

$$\phi_1(A)=\frac{e/2+C_gV_{g1}}{C_1+C_g+C_0} \tag{7}$$

is the approximate upper bound of the voltage across the entrance transistor. When V_{p1} starts falling and V_{p2} starts rising, the point moves from A to D in Fig. 4(b), whereas the point immediately reaches the unwanted border at E in Fig. 4(c) and moves along the border. This means that electrons are tunneling from node3 to node2 through TR3. At D, the point is pinned and electrons flow from node1 to node2 through TR2. Next, the point moves from D to F and electrons move from node2 to node3 at F. This time no unwanted tunneling occurs because G has not been reached in Fig. 4(d). Finally, the point goes to the last pinning point H and electrons are drained off node3 through TR4. Similarly to A, we see that

$$\phi_3(H)=-\frac{e/2-C_gV_{g4}}{C_2+C_g+C_0} \tag{8}$$

is the approximate lower bound for ϕ_3.

The reverse-direction tunneling reduces the net current, and therefore should be prevented. With regard to the edge transistors, B and G should not be reached to prevent the reverse flow, whereas A and H should be for successful pumping. This tells us that V_{g1} should be negative and V_{g4} should be positive. Better still,

$$-\frac{e}{2C_g}<V_{g1}<-\frac{e}{C_g}\left(\frac{1}{2}-\frac{C_2}{C_\Sigma}\right) \tag{9}$$

and

$$\frac{e}{C_g}\left(\frac{1}{2}-\frac{C_1}{C_\Sigma}\right)<V_{g4}<\frac{e}{2C_g} \tag{10}$$

should be satisfied for smaller $|\phi_1(A)/\phi_1(B)|$ and $|\phi_4(H)/\phi_4(G)|$. The overlap of the clock pulses helps to keep the state point from reaching B and G by moving the point to the next transistors' forward-direction borders. More intuitively, the falling pulse pushes electrons out of the present node, and the rising pulse pulls in the electrons to the next node. As for other transistors, the trajectory should not touch a border in the $\phi_i-\phi_{i+1}$ plane when ϕ_i increases, as in Figs. 4(b) and 4(c). This will prevent tunneling in the unwanted direction through the corresponding transistor. But the trajectory should reach a border while ϕ_{i+1} increases. This leads to tunneling in the favorable direction. Whether these conditions are fulfilled depends on the choice of V_{g1} and V_{g4} as well as on the position of stability rhomboids in

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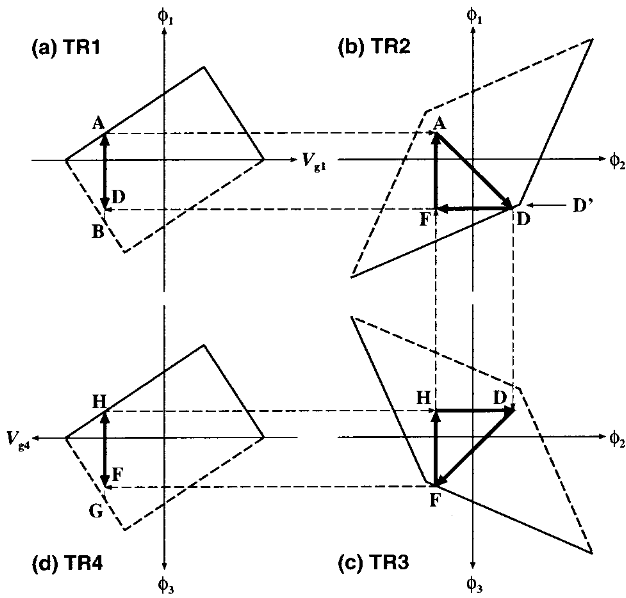

FIG. 5. Steady trajectories for well-chosen V_{g1} and V_{g4} at $T=0$ K. $V_{g2}=V_{g3}=0$ V. The state point draws triangles in the $\phi_i-\phi_{i+1}$ planes.

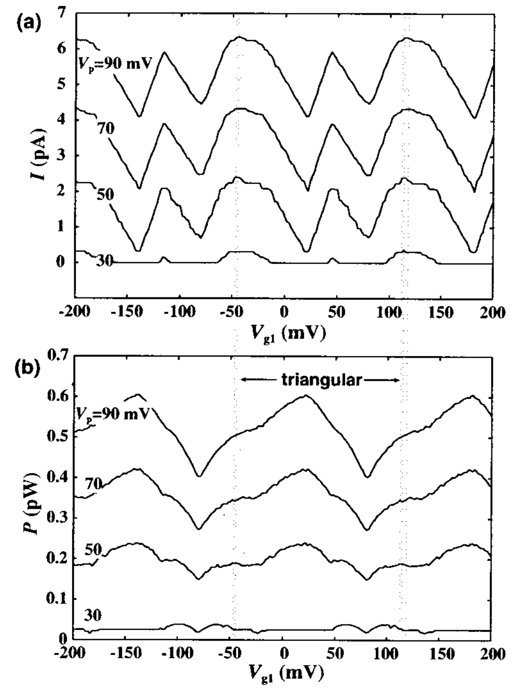

FIG. 6. (a) Net current I and (b) power P as a function of V_{g1} for different values of clock amplitude V_p. The triangular condition occurs at around current maxima, e.g., $V_{g1}=-42$ mV. $V_{g4}=42$ mV, $V_p=100$ mV, $f=1$ MHz, and $T=0$ K.

the $\phi_i-\phi_{i+1}$ planes [Fig. 2(b)]. We will simply leave the rhomboids at the center by setting V_{g2} and V_{g3} to zero, and change only V_{g1} and V_{g4}. It should be noted that no clock pulse pushes electrons from the ground into node1 while V_{p1} rises nor does it pull electrons out of node3 to the ground while V_{p3} falls. The edge transistors therefore require special consideration.

Figure 5 shows the steady trajectories for a set of well-chosen V_{g1} and V_{g4}. While the state point is moving from D to A in Fig. 5(a), the point is always within the stability region for TR2 as shown in Fig. 5(b). As a consequence, electrons flow into node1 only through TR1 at A. Unlike in Fig. 4(b), the slope of the next segment of the trajectory, AD, in Fig. 5(b) is $-45°$ because no transistor is conducting. Subsequently electrons flow through TR2 at D, next through TR3 at F, and finally through TR4 at H. Thus electrons are almost perfectly rectified in this case, and therefore it is an optimal operation condition. In this condition, the trajectories in $\phi_i-\phi_{i+1}$ planes are isosceles right-angled triangles, so we will call it the ''triangular condition.'' In this case, only one transistor is conducting at a time, which means that packets of N_c electrons are indeed conveyed in the pump.

The net current and the power are plotted as a function of V_{g1} in Figs. 6(a) and 6(b), respectively. The triangular condition occurs around the current maxima, where the power is not maximal. Although the power is not minimal in that condition, the net current flows only in the triangular condition when the clock amplitude V_p is small. One should therefore use the triangular condition and smaller V_p to reduce the power. Otherwise, the pump will consume extra energy in vain.

The triangular condition also facilitates the estimation of N_c and the power from the circuit parameters because tunneling events are localized to a particular transistor at each moment. By virtue of the perfect rectification, N_c equals the number of electrons which enter the pump through TR1. Therefore

$$N_c \approx \{V_p-[\phi_1(A)-\phi_1(D)]\}/\delta\phi, \tag{11}$$

where $\phi_1(A)$ is given by Eq. (7) and $\delta\phi \approx e/C_G$. Pinning points like D in the $\phi_i-\phi_{i+1}$ planes are determined self-consistently. It is not straightforward to find the steady trajectories from a given set of side-gate biases. However, $\phi_1(D)$ may be approximated to $\phi_1(D')$.

$$\phi_1(D')=\frac{-(C_1+C_g+C_0-C_2)e/2}{(C_1+C_g+C_0)(C_2+C_g+C_0)-C_1C_2}. \tag{12}$$

The simulation gives $N_c \simeq 45.4$. Using Eqs. (7), (11), and (12), we obtain $N_c \simeq 46.7$, which is in good agreement with the simulation.

Since only one transistor becomes conducting at a time and $N_c e$ is the charge that passes through it, the power consumption due to tunneling is given by

$$\begin{aligned} P &= f\times N_c e \times \sum_i V_{\text{diff}}^{(i)} \\ &= fN_c e\{\phi_1(A)+[\phi_2(D)-\phi_1(D)] \\ &\quad +[\phi_3(F)-\phi_2(F)]-\phi_3(H)]\}, \end{aligned} \tag{13}$$

where $V_{\text{diff}}^{(i)}$ is the voltage drop across the ith transistor when it is conducting [cf. Eq. (1)]. By making use of Eq. (12),

$$\phi_2(D)-\phi_1(D)\approx\frac{2(C_g+C_0)e}{(C_1+C_g+C_0)(C_2+C_g+C_0)-C_1C_2} \tag{14}$$

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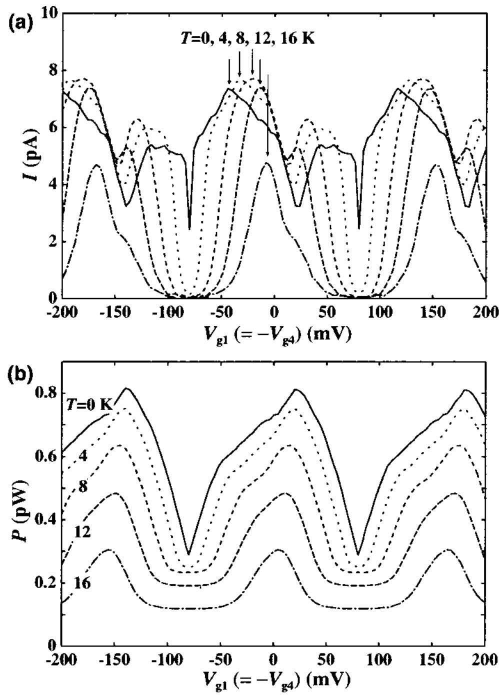

FIG. 7. (a) Net current and (b) power vs $V_{g1}(=-V_{g4})$ for various temperatures. $V_p=100$ mV and $f=1$ MHz.

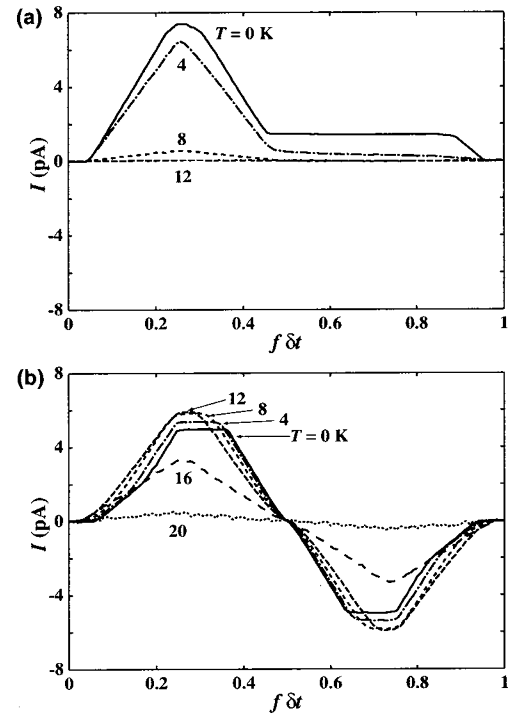

FIG. 8. Net current vs normalized phase delay $f\delta t$ for different temperatures. See also Fig. 1(c). $V_p=100$ mV and $f=1$ MHz. (a) $V_{g1}=-42$ mV, $V_{g2}=0$ V, and $V_{g3}=42$ mV, which gives the triangular condition at $T=0$ K. (b) $V_{g1}=V_{g2}=V_{g3}=0$ V.

and the same for $\phi_3(F)-\phi_2(F)$. Thus we can estimate the power to be $P\simeq 0.6$ pW. The simulation result is also $P\simeq 0.6$ pW. We note that Eq. (14) is a slight overestimate, whereas the simulation result includes the energy dissipation due to charging and discharging of capacitances.

The charge transfer mechanism in pumps with more transistors can be understood in the same way as the four-transistor pump. Steady trajectories in the $\phi_i-\phi_{i+1}$ planes become triangles at almost the same edge-transistor side-gate biases as the four-transistor case, and the approximation method presented above is also applicable *mutatis mutandis*.

Although we have only tried adjusting side-gate biases of the edge transistors, one could further improve the pump operation by changing the capacitances of the edge transistors. For instance, as regards TR4, asymmetry of the rhomboid about the V_1 axis increases by making $C_1<C_2$. This leads to lesser $|\phi_4(H)/\phi_4(G)|$, as can be seen from Fig. 3(a). Fine tuning of circuit parameters therefore is also an option worth exploring if sufficiently accurate fabrication technology is available.

V. TEMPERATURE AND FREQUENCY LIMITS

The main effect of nonzero temperature on the pump operation is to cause unwanted leakage current. At higher temperatures, the trajectories of a state point are no longer as simple as those in Figs. 4 or 5, and it is difficult to make good use of them. Qualitatively, stability rhomboids effectively shrink with temperature, so that the side-gate biases of the edge transistors that give a maximal current tend to shift toward zero, i.e., the middle of stability rhomboids. The magnitude of the effective shrinkage increases rapidly with T, as ΔF that gives the same leakage rate grows very quickly; see Eq. (4). The current is plotted in Fig. 7(a) as a function of $V_{g1}(=-V_{g4})$ for different temperatures. The current maxima approach $V_{g1}=-V_{g4}=0$ V as the temperature rises. At higher temperatures, some energy is supplied from the environment, so that the power consumption decreases as expected, which is shown in Fig. 7(b).

Figure 8 shows the current in a three-transistor pump circuit as a function of the normalized phase delay $f\delta t$ [see Fig. 1(c)] for two sets of side-gate biases for the edge transistors, namely V_{g1} and V_{g3}. In their experiment, Tsukagoshi *et al.* found $f\delta t=0.25$ to be optimal.[7] They also observed both positive and negative currents as they changed the phase delay. Figure 8(a), which is in the triangular condition at $T=0$ K, indicates the strong rectification in that condition, positive current is seen even with nonoptimal phase delay. However, as the temperature becomes higher, the net current vanishes rather quickly. With zero side-gate biases, current continues to flow up to much higher temperatures as shown in Fig. 8(b). The higher temperature results are in good agreement with the experimental results of Tsukagoshi *et al.*[7] We suppose the experiment was carried out in this regime, where the temperature was not very low and the side-gate biases were near the middle of stability rhomboids.

The two characteristic temperature scales involved in the pump are $e^2/2C_\Sigma k_B\simeq 170$ K and $e^2/2C_G k_B\simeq 9$ K. The highest operation temperature is determined not by the small island capacitance C_Σ of the MTJ transistors but by the comparatively large clocking-gate capacitance C_G. This is because the state point spends much of the time around the

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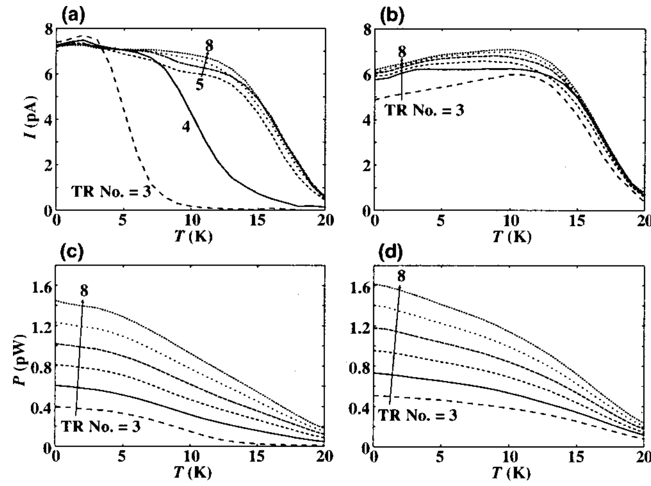

FIG. 9. Current and power vs temperature for different numbers of transistors in a pump. (a) and (c) are in the triangular condition at $T=0$ K. For (b) and (d) all side-gate biases are 0 V.

pinning points where the energy barrier for unwanted tunneling is of the order of $e\delta\phi$.[10] Figure 9 plots the current and the power versus temperature for pumps with different numbers of transistors. Figures 9(a) and 9(c) are in the triangular condition at $T=0$ K and Figs. 9(b) and (d) are with zero side-gate biases. Again, zero side-gate biases tend to give more current at higher temperatures. The results confirm that the highest operation temperature is determined by C_G. Given the relative insensitivity to the temperature and to the transistor number seen in Fig. 9(b), the zero side-gate bias operation is a reasonable choice.

Too high a clock frequency f leads to missed tunneling events. After a state point has crossed a stability border, there is a finite time delay before tunneling takes place. At moderate frequencies, the delay is less than the time it takes ϕ_i to change by $\delta\phi$, which we write as $t_{\delta\phi}=(\delta\phi/V_p)\times(1/4f)$. If the delay is comparable to or longer than $t_{\delta\phi}$, a pump cannot fully follow the clock signals and the pumping operation deviates from ideal.[10] The upper frequency limit $f_{\max}$ for vanishing temperatures can be estimated as follows. The time delay approximates to the inverse of tunneling rate Γ^{-1}. It is convenient for the present purpose to express ΔF in the form $\Delta F=-e(V_i+V_f)/2$, where V_i and V_f are the voltages across the tunnel junction before and after tunneling, respectively. In our case, $V_{i,f}\approx\pm e/2C_\Sigma$, and at a sufficiently low frequency $V_i+V_f\rightarrow 0$. In the higher frequency range we are interested in, $V_i+V_f\approx\delta\phi$, and hence $\Delta F\approx -e^2/2C_G$. Using Eq. (4) and $I(V)=V/R_T$ under $k_BT/\Delta F\ll -1$,

$$\frac{1}{t_{\delta\phi}}=\frac{4V_pf_{\max}}{\delta\phi}\approx\Gamma=\frac{\delta\phi}{2eR_T}. \tag{15}$$

We therefore obtain

$$f_{\max}\approx\frac{e}{8V_pR_TC_G^2} \tag{16}$$

as a rough estimate of the frequency above which the pump operation is expected to degrade. The numerical value for our simulation is $f_{\max}\approx 1\times 10^8$ Hz, roughly above which the current does not increase linearly with f, as confirmed in Fig. 10(a). We add that the threshold frequency depends on side-gate biases.

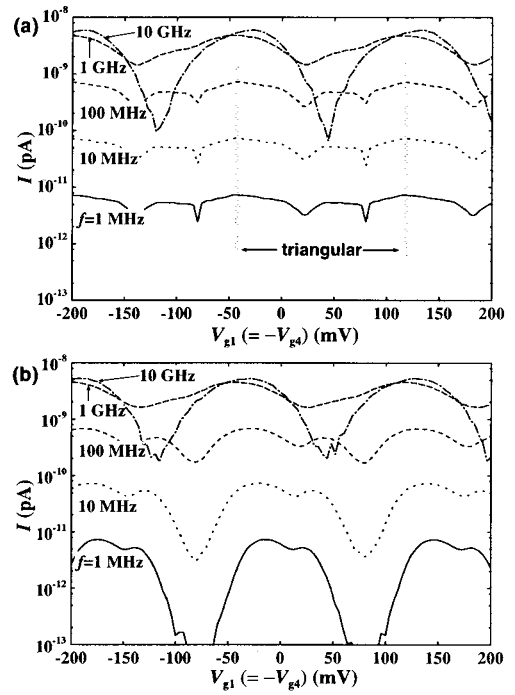

FIG. 10. Frequency dependence of the pump current. (a) $T=0$ K. (b) $T=12$ K.

At nonzero temperatures, the delay becomes shorter and thermally activated tunneling (with $\Delta F>0$) also occurs. Thermal errors affect pumping more at low frequencies,[10] and it is seen as deeper current troughs in Fig. 10(b) at low f. The upper frequency limit does not differ significantly from that for the zero-temperature case.

VI. DISCUSSION

We have investigated the operation of multiclocked pumps using a simplified model, assuming rather idealized situations, such as the uniformity of the pumps. We have derived approximate formulas which enable one to evaluate the number of electrons transferred per clock cycle and the power dissipation from a given set of circuit parameters. Because of the restrictions imposed, our approximation method might be more useful as a means of estimating the best possible performance achievable by such pump circuits, rather than as a means of understanding the details of nonideal, experimental results.

The estimated operation temperature and frequency are not particularly high even with the relatively optimistic numerical values used in the simulations. The power consumption, on the other hand, is very low. This is because of the small number of electrons involved and the low operation voltage. Operation with a much higher clock frequency, e.g., $f_{\max}$, is perfectly acceptable in this capacitance range, as far as power is concerned. If the entire circuit is scaled down with keeping the ratio C_Σ/C_G constant, higher values of temperature and frequency would be achieved in theory. However, the scaling also means operation with accordingly

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higher voltages. Specifically, $V_{\rm diff}^{(i)}$ in Eq. (13), which reflects the size of the stability rhomboids, becomes larger. Consequently, the power consumption increases by the scaling if f and N_c are held constant. If the voltage and the frequency become comparable with those used in conventional circuits, the difference in power consumption would essentially arise from the difference in the amount of charge used, i.e., $N_c e$ in Eq. (13) and q in Eq. (1). Since we can make $N_c e \ll q$ by reducing the clock amplitude V_p, the pump circuits have an advantage over conventional circuits in this regard. Of course, whether such miniaturization is possible is another issue. Also, we did not consider the change in R_T by scaling down.

With respect to the BDD logic application, it is hoped that only one electron packet is sufficient as the medium of bit information, thereby realizing a high throughput. In fact, in the logic operation experiment reported by Tsukagoshi *et al.*, a large number of packets were used because of the very slow logic operation speed.[13] We found by simulation that it takes several cycles for a pump to settle into a steady trajectory. Furthermore, the longer the pump is, the longer it takes to settle. This might imply a possible difficulty with the single-packet operation scheme. Further study with an appropriate model of the switching device is needed to explore the prospects for an efficient logic application.

ACKNOWLEDGMENTS

The authors thank Professor H. Ahmed and Dr. K. Tsukagoshi for support and discussions. S. A. thanks Professor K. Hoh for support. This work was carried out under the management of FED as a part of the MITI R&D of Industrial Science and Technology Frontier Program (Quantum Functional Device Project) supported by NEDO.

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