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Fabrication of MOS–integrated metallic single electron memories

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The fabrication of a lateral single electron memory (LSEM) based on the integration of a metallic multiple tunnel junction (MTJ) and a memory node (MN) on a Si metal oxide semiconductor field effect transistor (MOS) has been investigated. High resolution electron beam lithography (HREBL) was used to fabricate devices presenting good morphological characteristics. The MN can be made as narrow as 50 nm, with an MTJ comprising a 5x5 array of sub–5 nm Au islands deposited by thermal evaporation, and implemented on a short 0.5 μm channel MOS. An operating temperature close to 77 K with the two memory levels relying on the excess or shortfall of approximately 30 electrons is expected.

1. INTRODUCTION

Single electron devices exploiting the Coulomb blockade effect present potential applications for ultra high density memory integration. In the single electron memory architectures proposed by Yano et al. [1] and Nakazato et al. [2], the memory node (MN) element, on which a controlled number of electrons can be stored, needs to be connected to an external electrode through a non–linear resistance, in order to obtain a hysteresis behaviour exploitable for memory application. A multiple tunnel junction (MTJ) exhibiting clear Coulomb blockade effect with a high enough voltage threshold can provide an effective non–linear element. Following this proposal, Stone and Ahmed [3] recently achieved a memory cell using a MTJ created by the non–uniform potential distribution occurring in a narrow etched Si wire. Although fully compatible with CMOS technology, this device is limited to low temperature operation (4.2 K). Alternatively, granular film deposition can be used to produce MTJs working at higher temperatures [4–6]. MTJs made of 2D arrays of disordered sub–5 nm metal islands, exhibiting reproducible Coulomb blockade behaviour at high temperature (>100 K), have been fabricated and characterized [5]. In this work we consider the next step towards the fabrication of a lateral single electron memory (LSEM): the integration of a metallic MTJ and a memory node (MN) on a Si metal oxide semiconductor field effect transistor (MOS). We are investigating a novel lateral memory cell architecture, where the electron trap is located on top of the MOS channel. The MN voltage differences, related to the charging or discharging of the MN through the MTJ during writing operation, can modulate the drain–source current of the MOS, which is used as a charge sensor in the reading operation.

2. FABRICATION PROCEDURE

A schematic top view of our single memory cell

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architecture is shown in Figure 1. The MTJ array connects the MN to the word line. Since the voltage changes in the small MN are not sufficient to induce an inversion layer in the full length of the underlying MOS channel, an additional split–gate, which is biased when the memory cell is to be read, is fabricated close to the MN.

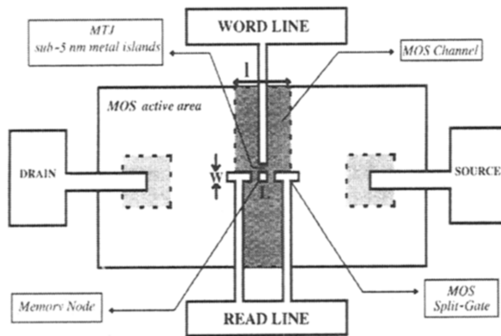

Figure 1. Simplified top view of the LSEM cell architecture

The conventional MOS structures processed have channel lengths l varying from 5 μm to 0.3 μm and a gate oxide thickness of about 7 nm. Doping levels have been chosen to obtain a threshold voltage around 0.5 V.

The memory cell is then completed using high resolution electron beam lithography (HREBL) on PMMA resist and Al lift–off. Two HREBL tools have been used in parallel. The first one is a 50 keV JEOL nanowriter with a 10 nm probe and the second one is a modified TEM/STEM working at 200 kV with a 1 nm probe size.

The source and drain contacts are processed first, after a local etch of the gate oxide in dilute HF. Sintering of the Al contacts is then carried out at 420°C for 30 minutes. The word line, MN and split gate elements are fabricated in another HREBL step. Various sizes of MNs (length L and width w) and split–gates (width w), as well as various spacings between word line and MN, have been designed on each die. Next to each complete LSEM structure, two types of test devices are fabricated and can be characterized separately. The first structure is a simple full–gated MOS having the same dimensions as the MOS included in the corresponding LSEM (channel length l and gate width w). This device enables the characterization of the MOS at different temperatures (drain–source current amplitude, threshold voltage). This test structure is of critical importance, particularly since we fabricate effective channels of very small width (w<100 nm). The second device is a simple MTJ device, placed between the word line and another similar electrode. The interelectrode distance matches the word line–MN spacing on the corresponding LSEM structure. This test MTJ therefore allows accurate measurement of the Coulomb gap and its evolution with temperature. Only the two electrodes are fabricated in this HREBL step.

The 2D metal MTJ arrays are formed next, using a subtractive approach. First, an optimized Au granular film is deposited by thermal evaporation on the whole surface of the die. Then, HREBL using PMMA in the negative regime is carried out to define a thin line of resist between word line and MN. Using the resist line as an etch mask, ion beam etching (IBE) is subsequently used to form a 2D mxn MTJ array comprising m islands between word line and MN and n islands across. Etching time is short enough that all Au islands are removed elsewhere but that the contact pads are not significantly affected. After IBE, the insulating PMMA line can be kept on top of the MTJ for protection and does not affect electrical characterization.

3. RESULTS AND DISCUSSION

Typical LSEM devices obtained are shown in the scanning electron micrographs of Figure 2. In the top picture, taken prior to island deposition, the MN is about 150 nm(L) x 100 nm(w) and the spacing between the MN and the split–gate is about 30 nm.

After a detailed study of electron beam exposure conditions for both lithography tools, we were able to fabricate structures with different dimensions for the MN (from L=50 nm to 200 nm), the spacing between MN and word line (from 5 nm to 60 nm), and the proximity of the split–gate to the MN (typically between 10 and 30 nm).

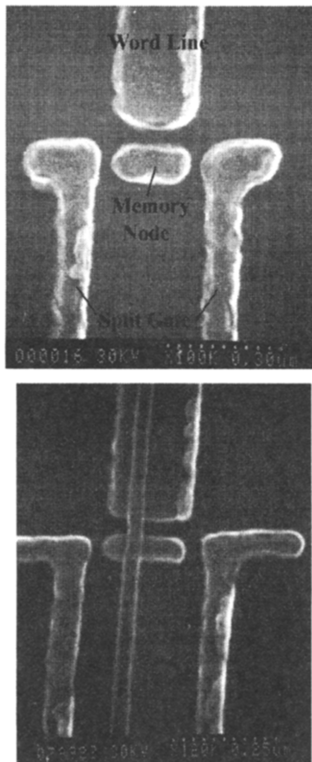

Figure 2. Example of fabrication of the MN element, split–gate and MTJ region. Top view: before island deposition, on a 0.5 μm–long channel MOS. Bottom view: after IBE using the central PMMA line as an etch mask, on a 0.6 μm–long channel MOS. The protected 2D MTJ array here comprises roughly 5x6 Au islands. Both devices were realized using the 50 kV JEOLnanowriter.

As we are working on rather short channel MOS structures (l down to 0.3 μm), accuracy of positioning of our gates on top of the MOS channel is a crucial issue. On the first processed structures, the alignment accuracy was not satisfactory. We thus designed new structures, including test patterns for the alignment, taking care of the possible field distorsions of the different patterning tools used between the initial MOS processing and our HREBL level. We now have a good alignment procedure both with the JEOL nanowriter and the TEM/STEM, and total placement accuracy of the MN/split–gate/word line unit on the MOS channel is slightly higher than 100 nm.

Precise alignment is again requested for positioning the negative PMMA line on top of the MN. Alignment accuracy is on average 30 nm for both our HREBL tools. An example of successful alignment of the resist line on the MN can be seen on the bottom micrograph of Figure 2. Since it is very important to avoid any conduction path between the word line and the split–gate, this alignment accuracy sets a limit for the minimal length of the MN element, which should therefore not be less than L=50 nm. However, there are no such restrictions on the width w of the MN, which can be made as small as 30 nm. The size of the MN fixes the number of electrons used to store the information. The minimal linewidth obtained for the negative PMMA line is roughly 30 nm as well. This linewidth sets the number n of islands comprised in the mxn MTJ array, while m depends on the word line–MN spacing. In the bottom picture of Figure 2, the size of the 2D array forming the MTJ is about 5x6 islands. MTJ arrays containing $1<m<10$ and $5<n<10$ islands are typically obtained.

A detailed study of island deposition conditions has allowed us to optimize the morphology of our disordered granular Au films and a high density of sub–5 nm islands with a 2 nm size dispersion could be reproducibly obtained [7]. The factors of merit of MTJs for memory application are i) a total tunnel resistance in the MΩ range in order that the writing time related to the speed at which electrons can pass through the MTJ remain in the ns regime, and ii) a clear conservation of a Coulomb gap at operating temperature, which depends on the number, size and average charging energy of the islands forming the MTJ array. An experimental study of the temperature dependance of our disordered 2D MTJ arrays, supported by Monte Carlo simulations [5], showed that lateral patterning of the 2D arrays made the devices more robust against temperature. Figure 3 shows typical current–voltage characteristics obtained on our 2D mxn Au MTJ arrays.

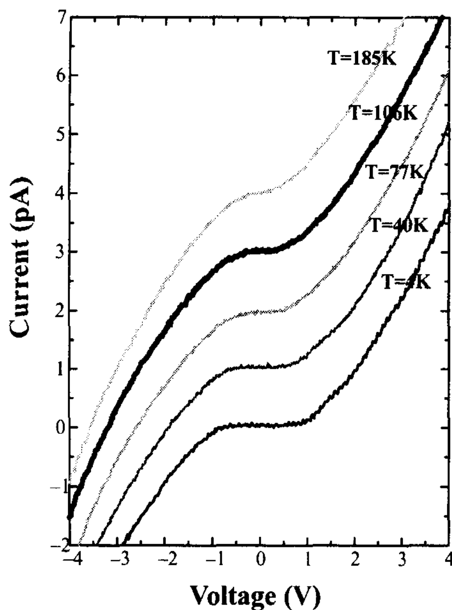

Figure 3. Typical I(V) characteristics obtained on our 2D mxn metal MTJ arrays at different temperatures. In the device shown here, m=8 and n=5. The curves were shifted for better understanding .

The large Coulomb gap measured at 4 K decreases with increasing temperature. Above a critical temperature, slightly higher than 100 K, the gap is destroyed and a conductance can be measured at low voltage [5]. The 1 V Coulomb gap obtained for the MTJ at low temperature should enable high temperature operation of the LSEM, as well as a modulation of the MOS current by more than 3 decades between the "0" and "1" states.

Therefore, for a 10 nm spacing between the MN and the split–gate, which is commonly achieved, our alignment accuracy only enables a minimal MN length of L=50 nm. On the other hand, the width of this MN, can be made as small as w=30 nm, thus giving a total surface of 1500 nm^2. These dimensions correspond to a total capacitance of about 10 aF for the MN element. As the threshold voltage commonly obtained in our MTJs is about 0.5 V at 4 K and 0.1 V at 77 K, it is then possible to predict the number of electrons storing the memory information. At 77 K this number corresponds to 30 electrons while it is reduced to only 6 electrons near 4 K.

4. CONCLUSION

We have fabricated split–gate LSEM structures with sub–5 nm metallic islands using HREBL and granular metal film deposition by thermal evaporation. The nanofabrication procedure has been optimized and our best structures typically comprise a MN 50 nm–long and 30 nm–wide, connected to the word line via a 5x5 MTJ array, and separated from the split–gate by 10 nm. According to our characterization of similar isolated MTJ devices and to our capacitance and LSEM calculations, we can expect our LSEM structures to work up to 77 K, with a number of electrons between 6 and 30 as a function of temperature, and a modulation of the MOS current between "0" and "1" states of 3 orders of magnitude. Electrical characterization of our LSEM devices has now started. These measurements should soon allow us to confirm the ability of our MOS structure to sense the small charge differences on the MN. We will also have access to the memory retention time as a function of temperature, as well as to the writing/erasing speed, which both depend closely on the total tunnel resistance of the mxn MTJ array.

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