Memory Cell Simulation on the Nanometer Scale

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Abstract—We describe a toolset of simulation programs and its use for the simulation of a memory cell based on Coulomb blockade. We present simulation results both for the main parameters of the memory cell and the influence of parasitic effects. We point out that both setting up specific programs and providing data exchange between them is necessary in order to describe the memory cell to a realistic extent.

Index Terms—FET memory integrated circuits, intelligent design assistants, memory architecture.

I. INTRODUCTION

THE GAIN-CELL concept as devised in flash memory paved the way toward the use of less charge per bit (e/bit, e = elementary charge) in electronic memory. In future this might lead to Coulomb blockade (CB) based memory cells using even less charge ($1 \cdots 1000\, e$/bit) and direct tunneling instead of Fowler–Nordheim tunneling.

In this paper we report on the simulation of a CB memory cell. This is a lateral single electron memory cell (LSEM cell) as shown in Figs. 1 and 2. It was proposed [2] recently and its operation was demonstrated [3]. The CB device of the demonstrated cell was a silicon multiple tunnel junction. However, a granular metallic film can be used instead, thus even simplifying the cell layout owing to the unnecessary trimming gate. The details of the working principle are outlined in Section II. Making use of a variety of simulation tools (Section III) we assess the potential of the LSEM concept and evaluate its value in terms of reliability. The resultant data are shown in Section IV.

We concentrate on new, unpublished, material, which demonstrates the interconnection of our simulation tools. We kindly refer the reader to the references for specific aspects of the simulation.
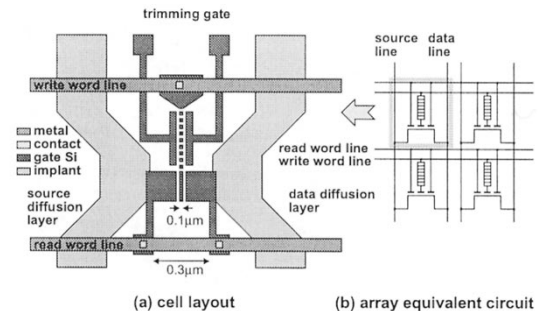
Fig. 1. Schematics of the suggested LSEM cell: (a) Layout of the cell, the CB device connects write word line and memory node for the write/erase process. The read word line implements a built-in row select. The memory cell is read out via the transistor beneath read word line gates and memory node (gain-cell operation). Crucial dimensions are the memory node width ($0.1\ \mu$m) and the source drain separation ($0.3\ \mu$m). (b) LSEM cell array illustrating the incorporated row select by means of the read word line.
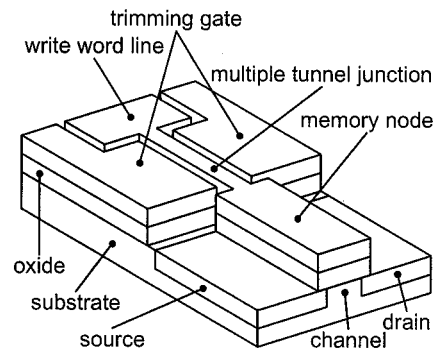

Fig. 2. Simplified layout of the LSEM cell without read word line as fabricated in SOI with extremely thin oxide ($\approx$20 nm).

II. LSEM OPERATION

The LSEM cell as shown in Figs. 1 and 2 belongs to the gain-cell type of memories. Fig. 2 provides an oblique view of an implementation in silicon on insulator (SOI). The read word line is left out for clarity. Write/erase uses the displayed write word line. Through a silicon multiple tunnel junction [4] charge is transferred to or from the memory node when an appropriate write word line voltage is applied. A trimming gate is used to control the working point of the multiple tunnel junction, the Coulomb blockade of which confines the charge on the memory node. The read out process uses a MOSFET that is implanted into the bulk silicon of the SOI wafer underneath the memory node and the read word line gates. This enables gain-cell operation, as the charge state of the memory node thus controls the current through the read out transistor. The read word line gates allow for an built-in row select.

III. SIMULATION TOOLS

A comprehensive simulation package for the LSEM cell consists of at least three parts: 1) capacitance simulation, 2) device level simulation, and 3) circuit level simulation. In order to model the fabrication of CB devices the simulation package has to be supplemented by corresponding process simulation software. Full-feature I–V characteristics of CB devices using an

orthodox lumped-element model also require a tunneling resistance model.

A. CB Device Simulation

Capacitance simulation is central to the understanding of CB devices since their characteristic energy scale, the charging energy E_c, is directly correlated via $E_c = e^2/(2C)$, where C is the capacitance of the electrode under consideration [5]. For metallic systems, where the problem is merely a computational one, the FastCap program[1] enjoys the status of a quasi standard, but new theoretical/numerical approaches [6] and commercial programs are emerging. For semiconducting systems, namely quantum dots, the computation is much more involved and a challenge in itself [7].

Our capacitance simulation is based upon an analytical formula for homogeneously charged rectangular electrodes. [8] Larger, irregular, inhomogeneously charged, but still planar electrodes can also be assembled. Accuracy problems arising from the use of very small cells can be addressed by a higher-order expansion of the original formula, [9] but similar problems persist for cells with large aspect ratio. The common plane of the electrodes is considered to be sandwiched between two semi-infinite dielectrics. Despite the limitation of the approximation as well as the computation time for large systems, the method yields realistic results for both metallic [10] and semiconducting [11] systems.

The output of the capacitance computation is the complete capacitance matrix for the structure including the self-capacitance of each electrode, which allows for an estimate of the corresponding stray capacitance. The capacitance setup describes the electrostatic interaction of the macroscopic system.

Together with a model of the resistance, it is possible to compute a current through a CB device in an orthodox lumped-element scheme. The resistance is a tunneling resistance and thus depends strongly on the characteristics of the tunneling barrier. The values obtained were found to vary considerably with slight changes of the barrier parameters and are generally less reliable than the capacitance computation. Nevertheless, a number of resistance formulae for different systems exist [13]. For metallic systems we have used a recent approximation [14] to simulate the current through a granular film [15].

B. Device Level Simulation

An important point in the LSEM cell design is the coupling from the CB part of the cell to the more standard parts. For our specific example, the coupling is achieved by the memory node, which is charged and discharged via a lateral CB device and whose charge state is sensed by a MOSFET underneath. Device level simulation is employed to study this coupling as well as corresponding parasitic effects. Furthermore, estimates of the selectivity of the memory cell rely on device level simulation.

In the case of the LSEM cell, commercial device level simulation (Atlas v4.0.3.R, © Silvaco International, Inc.) is sufficient due to the macroscopic, however still sub-μm size of the memory node. Depending on the operation principle of the memory cell this might not hold for a different memory concept.

For CB memory structures, which probably will have to rely on gain-cell operation and—therefore—incorporated MOSFETs, the advantage of memory node coupling of the LSEM cell is evident. Therefore, the approach presented here is rather general.

C. Circuit Level Simulation

Conventional circuit level simulation is usually SPICE based. Therefore, it became very attractive to connect the simulation of CB devices [16]–[19] with a SPICE simulator as achieved recently [20], [21]. Whereas for simple CB devices, like the single electron transistor, the direct solution of the orthodox master equation [22] provides an efficient means for an accurate computation of the tunneling current as well as conductance, more complex setups have to rely on Monte Carlo techniques [17] which have an intrinsic difficulty in providing smooth differential conductance data and thus complicate co-operation with the SPICE environment. However, these problems were addressed and—to some extent—solved recently [20], [21].

IV. RESULTS

For different reasons we select only a few results for discussion in this section. First, a fair amount of work on specific parts of the memory cell simulation has been published in recent years. Second, the emphasis of this paper is rather on the interconnection of different simulation tools than specific aspects of the simulation.

Therefore, our main example uses CB simulation to extract the blockade voltage V_b from the geometry of the CB device. This parameter is then used in a device level simulation to tune the outer voltage regime (read/write process) and dynamic behavior of the memory cell. In our case, the contents of the memory cell is read via the transistor current. This value enters, for instance, the sense amplifier simulation, where it determines the value of the input resistance or the corresponding voltage V_{res} (Fig. 6).

A. CB Device Simulation

The hysteresis of the employed CB device is a cardinal point of the LSEM operation. Therefore, simulation of the CB device has a significance in its own right.

The LSEM cell as presented in Section II contains a silicon multiple tunnel junction as CB device. First simulation results for this system were presented recently [23], [24]. For the layout using a granular metallic film—as mentioned above—exist corresponding simulations [15].

An important parameter of the CB device is its blockade voltage V_b, which depends upon the capacitance matrix [25] and the background charge constellation. By combining capacitance computation and current simulation one can already evaluate important reliability issues like the influence of disorder on the blockade voltage V_b [12]. Due to their stochastic nature, disorder effects have to be studied on the basis of averages using large ensembles. It is found that disorder in general leads to a wider distribution of the V_b values and might—in case of background charge disorder—even produce a CB breakdown [12].

In the latter case, which is still a topic of lively scientific discussion, we find that multiple tunnel junctions provide some immunity to background charge disorder. Only specific, partly coherent, and therefore highly unlikely patterns of these charges result in a complete breakdown of CB. On the other hand, there are also patterns of background charges which cause actually an increase of V_b, i.e., if they alternate along the current direction.

Of course, a CB breakdown would prohibit the memory cell operation, but also too wide a V_b distribution would hinder an application since $(V_{\mathrm{wrd}} - V_b)$, V_{wrd} being the write word line voltage, influences the write time exponentially [26]. The design goal is therefore a sharp V_b distribution. The average of this distribution can be used to estimate the operation temperature via $10k_BT \approx e\,V_b$. Our results for 5 nm dot yield an operation temperature of about 30K and require size control of ± 1 nm [12].

The consideration of the tunneling resistances and the related computation of full I–V characteristics is easier to achieve for metallic than for semiconducting systems since the free electron model can be used [13]. This was demonstrated recently [15] using a model closely linked to experimental data [14].

In the case of semiconducting CB devices the problem can be circumvented by the use of *a priori* resistance values which can be stepped through a reasonable range [26]. This allows for the evaluation of the write/erase process as outlined in Section II in terms of speed and stability. A complete set of timing diagrams for the different operations exists.

B. Device Level Simulation

Mainly, device level simulation is useful for the optimization of the memory cell layout. In some cases a simple capacitance calculation already provides interesting data. In Fig. 3, we display the number of electrons used for coding one bit of information as a function of the memory node geometry. This parameter is important for the comparison with conventional dynamic random access memory (DRAM) $\approx 10^5 e$/bit) and flash memory ($\approx 10^4 e$/bit) since it is strongly related to the power consumption. The simulation uses the blockade voltage V_b of the CB device as an input parameter, which in turn can be obtained from a CB device simulation similar to those in [12].

A standard example of device level simulation is the study of the read out process as a function of the read out transistor geometry as shown in Fig. 1 [2]. Some design parameters, like the gate oxide which is the oxide layer of an SOI wafer, are constrained by the technology. For others, there exist tradeoffs. One example is the memory node width. A wide memory node at the expense of the read word line gate width would cause slow charging and discharging. On the other hand, too small a memory node cannot shut off the transistor channel beneath and thus complicates the read out process. These questions are discussed in [2] extensively.

Another instructive piece of device level simulation is presented in Fig. 4, the (parasitic) coupling between read word line and memory node. The proximity of the "enable" gates of the read word line to the memory node causes a capacitive feedback. The task consists of two parts, the investigation of the charging process of the memory node and of the change of the obtained charge state as function of read word line voltage V_{rwl} and write word line voltage V_{wrd}.
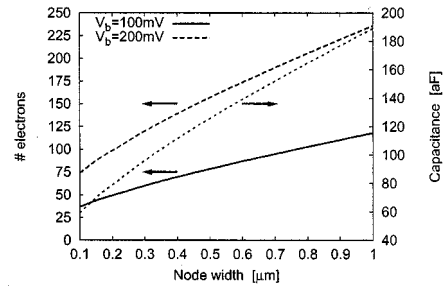

Fig. 3. Capacitance of the memory node of the LSEM cell and number of electrons on the node as function of the blockade voltage V_b for different memory node widths.
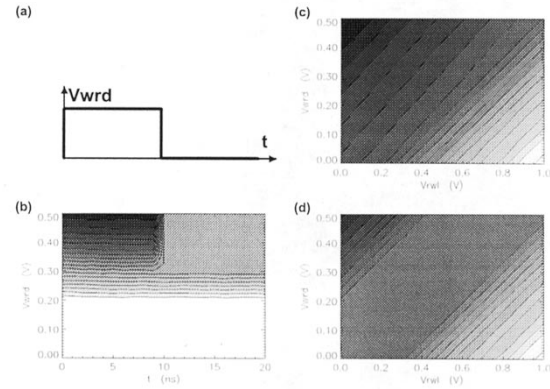

Fig. 4. Feedback of the read word line voltage onto the memory node charge: (a) A 10-ns voltage pulse of variable voltage V_{wrd} is applied to the write word line. In the following 10 ns the charge relaxation of the memory node is observed. (b) Corresponding memory node charge ranging from 0 (white) to 180 e (black). The blockade voltage is about 0.2 V and the memory node holds a maximum of about 80 charges. (c) After charging the memory node as shown in (a) and (b), both read word line and write word line are biased and the resultant memory node charge is plotted. Increasing read word line voltage depletes the charge state of the memory node. An increasing write word line voltage counteracts this process. The charge varies between $-290\ e$ (bottom right corner) and 190 e (top left corner). (d) Same as (c) for the equilibrium memory node. The same charge scale applies.

Charging of the memory node is shown in Fig. 4(a) and (b). For memory operation this corresponds to writing "1" into the memory cell. This is done by applying a voltage pulse of 10 ns to the write word line while keeping the read word line grounded [Fig. 4(a)]. Depending on the voltage of this pulse, V_{wrd}, three different scenarios are observed [Fig. 4(b)]. If $V_{\mathrm{wrd}} < V_b$ Coulomb blockade prevents charging of the node (in the displayed example: $V_b \approx 0.2$ V). For $V_b < V_{\mathrm{wrd}} < V_b + n_{\max}\ e/C_{\mathrm{node}}$, where $n_{\max}$ is the number of charges the memory node can hold if the leads are grounded ($n_{\max} \approx 80$) and C_{node} is the node capacitance ($C_{\mathrm{node}} \approx 130$ aF), charging of the memory node is proportional to $(V_{\mathrm{wrd}} - V_b)$. For even higher bias of the write word line, $V_{\mathrm{wrd}} > V_b + n_{\max}\ e/C_{\mathrm{node}}$ the memory node becomes over-charged during the voltage pulse, but its charge relaxes to $n_{\max}$ as soon as the bias is switched off.

The charge on the memory node as a function of applied V_{rwl} and V_{wrd} after the charging procedure described above is shown in Fig. 4(c). For comparison, the same function without pre-charging is displayed in Fig. 4(d). Both figures show that it is the balance between V_{rwl} and V_{wrd} that determines the
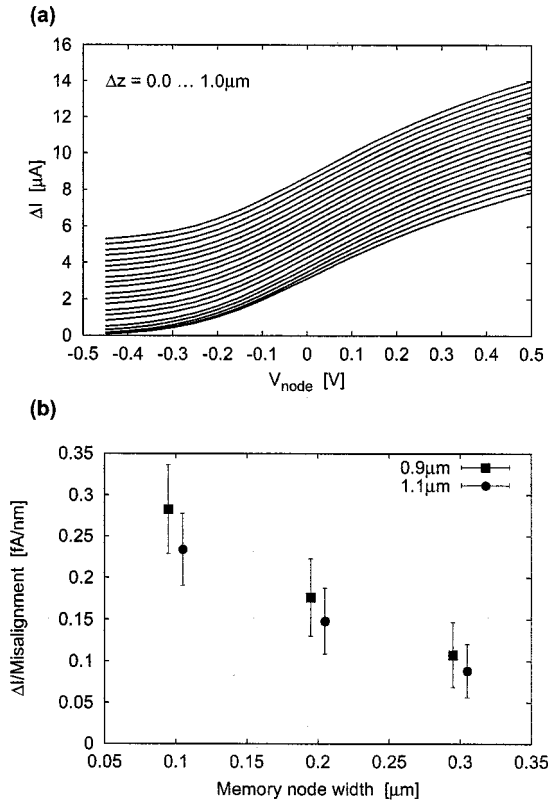
(a)

(b)

Fig. 5. Current through the read out transistor of the LSEM cell as function of the misalignment of memory node and read word line gate. (a) The current as function of the memory node voltage V_{node}. The read word line is enabled ($V_{rwl} = 0.2$ V) and the memory node width and implant separation are 0.1 μm and 0.9 μm, respectively. The misalignment increases from 0 (bottom) to 1 μm (top). (b) The parasitic current for different width of the memory node and different implant separation (0.5 μm misalignment).

memory node charge. The difference is the wide CB region of the uncharged node in Fig. 4(d), which prevents V_{rwl} from pushing charges back into the write word line and V_{wrd} from overcharging the memory node, similar to Fig. 4(a). If Fig. 4(c) displays state "1" of the memory cell and Fig. 4(d) "0" than we can learn from Fig. 4(c) that $V_{rwl} \approx V_{wrd}$ is the condition for preserving "1." V_{rwl}, $V_{wrd} < V_b$ is the similar condition for the "0" state. Therefore the read-out scheme [2] has to rely on sufficiently small values of V_{rwl} [2].

In the fabrication of real LSEM, misalignment of the memory node and the read word line gates might occur. The estimate of the parasitic current due to this effect is another example of device level simulation, this time using the 3-D features of the simulation program. In Fig. 5(a) the transistor current is shown for an enabled read word line ($V_{rwl} = 0.2$ V) and different values of the misalignment ranging from 0–1 μm in steps of 50 nm. Misalignment Δz is the length difference between read word line gate and memory node. In principle there is also the case of negative Δz, however the small width of the memory node compared to the read word line gates prohibits a reasonable transistor current. Despite the case of very small misalignment, the effect is an additional parasitic current which cannot be controlled by the memory node. In Fig. 5(b) we plot this current in dependence of the memory node width and the implant separation for 0.5 μm misalignment. The parasitic current can be effec-
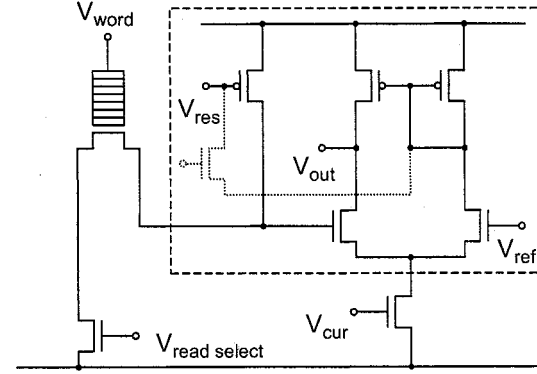

Fig. 6. Possible refresh organization for the LSEM memory cell. The top left corner displays the (simplified) memory cell. The dashed box contains the sense amplifier. The dotted refresh transistor communicates the reverse sense amplifier output to its input current converter, thus pulling up or down the data line.

tively suppressed by a wider memory node, but at the expense of the cell performance. There is also an effect of the implant separation, especially for a very narrow memory node. This is probably the better way to suppress the parasitic current.

C. Circuit Level Simulation

The LSEM circuitry simulation is a conventional SPICE simulation as far as the sense amplifier and other circuit elements are concerned. This part of the task is not presented in this paper. There are, however, cases where the combined simulation of the CB device and the read out transistor are important, and comprehensive simulation software [20], [21] becomes necessary.

One example is the simulation of the hysteresis curve of a single LSEM cell as presented in [23], [24]. These hysteresis curves shows additional features, i.e., steps, [3] which can be understood by use of comprehensive simulation and an appropriate model of the multiple tunnel junction. Not only the appearance of the steps is explained—replica of the integrated Coulomb oscillations—but also some of their detailed features. More negative voltage of the trimming gate (see Fig. 1) causes fewer, but larger steps. For fixed trimming gate voltage the step size increases with the write word line voltage.

Closer to current technology is the example of the memory cell refresh, which is one of the basic principles of DRAM operation. The operation is based on the fact that refresh is possible via the data line (refer to Fig. 1). For gain-cell based memory, like flash memory, the electrical separation between memory node and data line obstructs refresh which is usually no problem, since flash memory is a nonvolatile memory. The situation is different for the LSEM cell which generally is assumed to be relatively volatile [2]. Capacitive coupling between memory node and data line might provide a possible route to refresh in this case. This coupling works similarly to the parasitic read word line coupling discussed above, but uses the implanted data line instead of the read word line.

Fig. 6 shows a possible implementation. An additional refresh transistor is used to feed the sense amplifier output back onto the data line. For an appropriate value of the drain gate capac-

itance of the cell's read out transistor this might be sufficient to reestablish the original charge state of the memory node. A quantitative analysis of the operation has still to be performed.

V. CONCLUSION

The advent of Coulomb blockade (CB) based electronics requires new simulation tools and their cooperation with existing software. Using the example of a CB memory cell we illustrate this situation. In our discussion, we provide examples of cell design (memory node width), parameter extraction (number of electrons per bit), and error analysis (memory node misalignment). We show different cases of data exchange between programs from a single extracted parameter (blockade voltage) up to complex program interaction.

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