$InAs_{0.8}Sb_{0.2}$ channel material was grown at 400°C as a digital alloy superlattice with 10 periods of 4 ML InAs/1 ML InSb [2]. Modulation doping was achieved through the use of a thin Si-doped InAs layer located 125Å above the channel [3]. The sheet carrier density and mobility of the starting material at 300K were $1.4 \times 10^{12}cm^{-2}$ and $13{,}400cm^2/Vs$, respectively. The HEMTs were fabricated using Pd/Pt/Au source and drain ohmic contacts which were formed by heat treatment on a hot plate. A Cr/Au Schottky-gate was then formed using PMMA e-beam lithography and lift-off techniques. Finally, device isolation was achieved by wet chemical etching. With this etch, a gate air bridge was formed which extends from the channel to the gate bonding pad.

To confirm the type I alignment between AlSb and $InAs_{0.8}Sb_{0.2}$, we carried out photoluminescence (PL) measurements at 5K with a Fourier transform infra-red spectrometer. Samples were mounted on a cryogenic dewar and excited with an 810nm laser diode. The room-temperature blackbody radiation was eliminated by a double-modulation technique [4]. Fig. 2 shows the PL spectrum from the $InAs_{0.8}Sb_{0.2}$ single quantum well. In contrast to the nonluminous AlSb/InAs single quantum wells, this sample exhibits bright luminescence at 272meV. The arrow in Fig. 2 indicates the measured bandgap energy for a thick $InAs_{0.8}Sb_{0.2}$ digital superlattice. Our results imply that the lowest sub-band energy for a 150Å $InAs_{0.8}Sb_{0.2}$ quantum well is 62meV, consistent with $k{\cdot}p$ calculations.

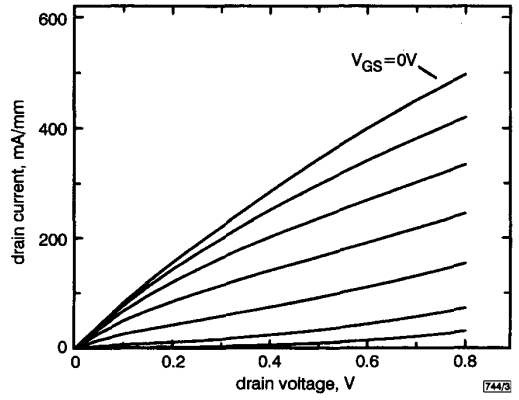

Fig. 3 *HEMT drain characteristics*
$L_G = 0.1\mu m$, $L_{DS} = 1.2\mu m$, $W_G = 100\mu m$, $V_{GS} = 0.1V$/step

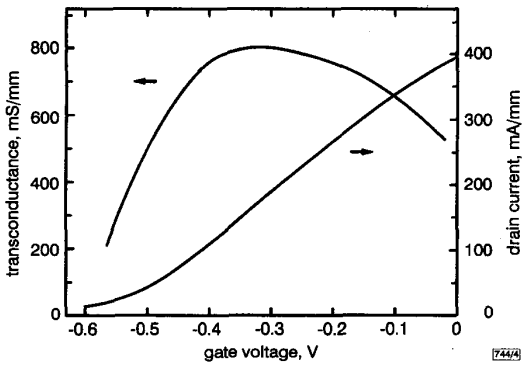

Fig. 4 *HEMT transconductance and drain current against gate voltage*
$V_{DS} = 0.6V$

The drain characteristics obtained for an HEMT with a 0.1μm gate length are shown in Fig. 3. The low-field source-drain resistance at $V_{GS} = 0V$ is 1.2Ω mm. The dependence of the transconductance and drain current on the gate voltage at $V_{DS} = 0.6V$ is shown in Fig. 4. A maximum transconductance of 800mS/mm is observed at $V_{GS} = -0.3V$. The S-parameters of the HEMTs were measured on-wafer from 1 to 40GHz. Based on the usual 6dB/octave extrapolation, an f_T of 130GHz and an f_{max} of 80GHz were obtained at $V_{DS} = 0.6V$ and $V_{GS} = -0.4V$. Using a simplified equivalent circuit, the microwave transconductance and output conductance for a 100μm gate width device are 700 and 110mS/mm, respectively, corresponding to a voltage gain of 6 at this bias condition. After subtraction of the gate bonding pad capacitance, an f_T of 180GHz is obtained. The highest f_{max} observed was 120GHz which was measured on a device with a 50μm gate width that had an output conductance of 50mS/mm and a voltage gain of 9. The output conductance and voltage gain are the best values reported for a 0.1μm antimonide-based HEMT. The improvement is believed to be caused by the confinement of holes in the channel as a result of the type I band lineup and the lower Δ-L valley energy separation which results in more saturation of the drain current. Improved high-speed performance should be possible with the addition of subchannel designs [3] which enable improved charge control and reduced impact ionisation.

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Silicon stacked tunnel transistor for high-speed and high-density random access memory gain cells

K. Nakazato, K. Itoh, H. Mizuta and H. Ahmed

Novel stacked tunnel transistors have been fabricated on silicon dioxide using a standard 0.2μm silicon process. From the measured characteristics it is shown that random access memory operations with 10ns read/write times are possible in cells which occupy the area of just one transistor.

Introduction: Dynamic random access memories (DRAMs) are used as the main memories in computers because of their high-capacity and high-speed. Since there is no gain in present DRAM cells, they require large cell-capacitors to produce sufficiently large sense signals. The structure and fabrication processes have become increasingly complicated so as to maintain the large capacitance while further miniaturising the cell in each new generation.

In this Letter we describe a novel stacked tunnel transistor which enables a new gain cell to be realised for high-density and high-speed random access memories [1]. Since this memory cell has gain, a large capacitor is not necessary. The memory cell is vertically structured, and effectively occupies the area of just one transistor. Simulations have indicated read and write times of 10 ns. In principle, it is possible with this cell to have a retention time of > 10 years [2], enabling a non-volatile memory with ultra-low voltage operation to be realised.

Transistor: The transistor is a vertical, fully depleted, double-gate SOI-MOSFET (silicon-on-insulator metal-oxide-semiconductor-field-effect-transistor) with barriers in the channel region, as shown in Fig. 1. The gate voltage modulates the internal potential

in the intrinsic silicon region and the central shuffer barrier (CSB) or barriers also move up and down energetically following the internal potential. The CSB reduces the OFF current substantially, while maintaining a high device ON current. The role of the source and drain barriers is to adjust the source impedance to the CSB to act as diffusion barriers keeping a low impurity level within the channel, and to reduce the leakage current such as the gate induced drain leakage current at the drain side.

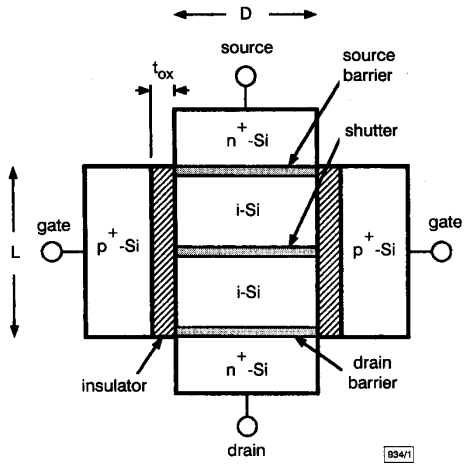

Fig. 1 *Stacked tunnel transistor*

Schematic cross-section of transistor fabricated with 60nm channel length and triple tunnel barriers

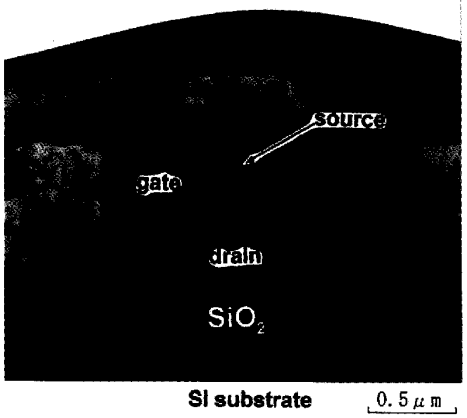

Fig. 2 *Transmission electron micrograph of transistor in Fig. 1*

The transistors with triple tunnel barriers were fabricated on silicon dioxide using a standard 0.2μm silicon process, as shown in Fig. 2. All transistor regions, source, drain, channel, and gate, are made from polycrystalline-silicon films. The thin tunnel junctions were formed by thermal nitridation of silicon; after deposition of the silicon layer, the surface of the silicon is directly converted to silicon nitride by heating at 900°C for 3min in a 100% NH_3 ambient. The thickness of the nitride is self-limited to ~2nm with a barrier height of ~2eV [3]. The source and drain regions were heavily phosphorus doped to 2×10^{20}cm^{-3}, and the channel region was maintained at a low impurity level, lower than 10^{18}cm^{-3} as confirmed by SIMS analysis. The gate was boron doped to 5×10^{19}cm^{-3}. The channel length L was 60 nm and the gate insulator was formed from 6nm of silicon dioxide. The gate separation width D was 0.2μm, and the gate width, perpendicular to the plane of Fig. 2, was 0.4μm on the optical photo-masks.

Drain currents were measured against gate voltage for several drain voltages as shown in Fig. 3. The leakage current was < 0.1pA, which is the limit of our measurement system. A subthreshold voltage swing S of 96mV/decade was obtained, which is explained well by the scaling theory for a double-gate SOI MOSFET [4] as shown in the inset of Fig. 3, where λ is the scaling length given by

$$\lambda = \sqrt{D^2/8 + Dt_{ox}\varepsilon_{Si}/2\varepsilon_{SiO_2}} \quad (1)$$

ε_{Si} and ε_{SiO2} are dielectric constants of silicon and silicon dioxide, respectively. TEM observation showed that the gate separation length D was 0.045μm as a result of over-etching the poly-Si, and $L/2\lambda$ is estimated to be 1.2. From scaling theory, the same characteristics can be obtained for 0.2μm gate separation length if the channel length is designed to be 200nm, and ideal subthreshold voltage swing of 60mV/decade will be obtained in long channel transistors.

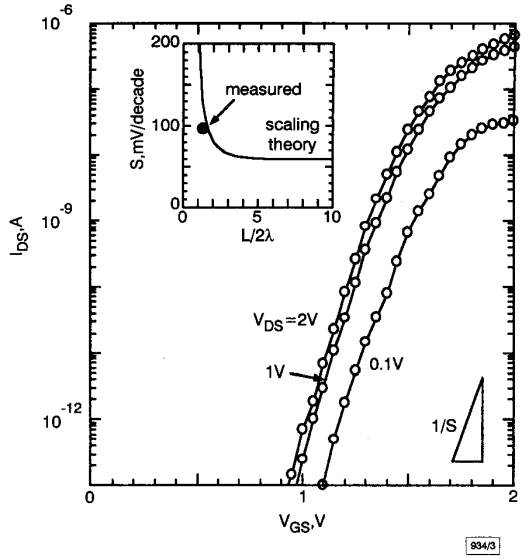

Fig. 3 *Measured drain currents at room temperature*

Inset: Subthreshold voltage swing against normalised channel length, comparing measured data and scaling theory

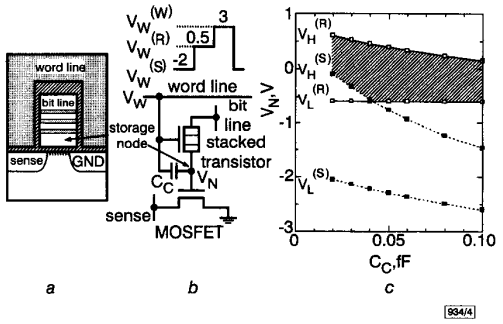

Fig. 4 *Cross-section of memory cell, equivalent circuit diagram and simulated memory node voltages*

$V_H^{(R)}$ and $V_L^{(R)}$ are in read cycle in high and low memory states, respectively; $V_H^{(S)}$ and $V_L^{(S)}$ are in storage cycle

a Cross-section

b Equivalent circuit

c Simulated node voltages

Gain cell: The transistor enables the construction of a novel high-density memory because each memory cell occupies the area of just one transistor, as shown in Fig. 4. The transistor is stacked onto the gate of a conventional MOSFET with a built-in coupling capacitor for random access in memory cell arrays. High-speed writing is made possible by 'cooler' electrons transferred from the top electrode (bit line) onto the storage node through the ON-state stacked transistor. Since the OFF-state stacked transistor can confine electrons very effectively, the stored information can be kept for a long time without a refresh operation. Since the information is read through a MOSFET, this cell has gain and a large S/N ratio. The cell also has a high degree of immunity against soft errors because the essential memory section is small and isolated from the substrate, since there are no floating body effects as in partially-depleted SOI devices, and because the tunnel barriers restrict the separation of electron-hole pairs.

The gain cell consists of a stacked transistor, a sense MOSFET, and a built-in coupling capacitor as shown in Fig. 4. Storage, read, and write cycles are all controlled by voltage V_W on the word line, $V_W^{(S)}$ (–2V), $V_W^{(R)}$ (0.5V), and $V_W^{(W)}$ (3V), respectively. In the storage cycle the built-in capacitor Cc leads to the memory node voltage being lower than the threshold voltage V_{th} of the sense MOSFET. In the read cycle the memory node voltage becomes higher than V_{th} when the memory state is high and lower than V_{th} when the memory state is low. In the write cycle the stacked transistor is opened, and the memory node voltages become the bit line voltages, 1.5V for the high memory state and 0V for the low memory state. Using the transistor characteristics of Fig. 3, for a mixed-level device, a circuit simulation for a 10ns read/write cycle was performed, and the memory node voltage V_N was calculated as a function of coupling capacitance Cc (Fig. 4). Random read access in the cell arrays is possible when V_{th} is set inside the hatched area, for example, between 0.5 and –0.5V at a coupling capacitance of 0.04fF. This coupling capacitance can be realised for a 50nm thick storage node, without needing to form an additional capacitor. Thus a memory cell size as small as $4F^2$ where F is the minimum feature size may be realised.

The stored charge is determined by the gate capacitance of the sense MOSFET, and estimated to be 0.2fC. Although the drain-source current in the ON state of a stacked transistor is small, ~1μA, high-speed writing can be realised because of the reduced stored charge. In fact, writing was performed within 1ns in this simulation.

Conclusion: Stacked tunnel transistors have shown good current-voltage characteristics with extremely low leakage current. Using this stacked tunnel transistor, a new RAM gain cell can be constructed with a one-transistor cell size and with 10ns read/write times. In principle, the retention time can be longer than 10 years in this cell, although several possible leakage mechanisms such as due to hopping conduction must be clarified.

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Asymptotic criterion for neutral systems with multiple time delays

Chang-Hua Lien

A delay-dependent criterion is proposed to guarantee asymptotic stability for uncertain neutral systems with multiple time delays. The criterion provides some information as to the size of time delays and is expressed by two inequalities. An example is given to illustrate the result.

Introduction: In recent years, the stability problem in time delay systems has been extensively investigated [1 – 7]. This is due to theoretical as well as practical interests for system analysis and design, since many engineering systems have inherent delay properties, such as nuclear reactors, rolling mills, ship stabilisation systems and systems with lossless transmission lines [1 – 3]. Delays frequently lead to instability and are a source of oscillations in many systems; for example, the trivial solution of $\dot{x}(t) + 2\dot{x}(t) = -x(t)$ is asymptotically stable, but that of neutral system $\dot{x}(t) + 2\dot{x}(t-\tau) = -x(t)$ is unstable for any positive delay τ [3].

Consider the linear system

$$\dot{x}(t) = \left[\sum_{i=0}^{m} B_i\right] x(t) = Bx(t) \qquad t \geq 0 \qquad (1)$$

where $x(t) \in \Re^n$, B_i, $B \in \Re^{n\times n}$, $i = 0, ..., m$. The necessary and sufficient condition for the asymptotic stability of the system of eqn. 1 is that $B = \Sigma_{i=0}^{m} B_i \in \Re^{n\times n}$ is Hurwitz (stable). It is reasonable to consider that the system contains state delays

$$\dot{x}(t) = B_0 x(t) + \sum_{i=1}^{m} B_i x(t-\tau_i) \qquad t \geq 0 \qquad (2)$$

where $\tau_i \geq 0$, $i = 1, ..., m$. Many delay-dependent criteria have been presented for evaluating the allowable delay magnitude for asymptotic stability of time-delay systems [4 – 6]. In the real world, systems will contain some information about past derivatives of a state [1 – 3, 7]. The aim of this Letter is to consider the delay-dependent criterion for the asymptotic stability of uncertain neutral systems with multiple time delays.

The notation used throughout this Letter is as follows. For a matrix A, we denote the standard Euclidean norm by $\|A\|$, the matrix measure by $\mu(A)$, and the determinant by $\det[A]$.

Stability analysis: Consider the following uncertain neutral system:

$$\dot{x}(t) + \sum_{i=1}^{m} \Delta A_i \dot{x}(t-\tau_i) = B_0 x(t) + \sum_{i=1}^{m} B_i x(t-\tau_i) \qquad t \geq 0 \qquad (3a)$$

$$x(t) = \phi(t) \qquad t \in [-\tau, 0] \qquad (3b)$$

where $x \in \Re^n$, x_t is the state at time t defined by $x_t(s) := x(t+s)$, $\forall\, s \in [-\tau, 0]$, $\tau = \max_i \tau_i \geq 0$, with $\|x_t\|_s := \sup_{-\tau\leq\theta\leq 0}\|x(t+\theta)\|$, $B_i \in \Re^{n\times n}$, $i = 0, 1, ..., m$, are known matrices, ΔA_i, $i = 1, 2, ..., m$, are constant perturbed matrices, and $\phi \in C$ is a given initial function, where C is a set of all continuous functions from $[-\tau, 0]$ to $\Re^n$. The following assumption is made for the system of eqn. 3 throughout this Letter:

A1: There exist non-negative constants α_i, $i = 1, 2, ..., m$, such that

$$\|\Delta A_i\| \leq \alpha_i$$

Lemma 1: For matrices ΔA_i, $B_i \in \Re^{n\times n}$ satisfying A1, if $\Sigma_{i=1}^{m}[\alpha_i + \tau_i \cdot \|B_i\|] < 1$, then the operator D: $C \mapsto \Re^n$ with $D(x_t) = x(t) + \Sigma_{i=1}^{m}[\Delta A_i x(t-\tau_i) + B_i \int_{t-\tau_i}^{t} x(s)ds]$ is stable [1].

Proof of Lemma 1: The characteristic equation of homogeneous equation $D(x_t) = 0$ is

$$\det[\Delta(z)] = \det\left[I + \sum_{i=1}^{m}\left(\Delta A_i \cdot e^{-z\tau_i} + B_i \cdot \int_{-\tau_i}^{0} e^{zs}ds\right)\right] = 0 \qquad (4)$$

Note that

$$\sum_{i=1}^{m}\left[\Delta A_i e^{-z\tau_i} + B_i \int_{-\tau_i}^{0} e^{zs}ds\right] \leq \sum_{i=1}^{m}(\alpha_i + \tau_i\|B_i\|) \qquad \forall\, \mathrm{Re}\, z \geq 0$$

Hence the condition $\Sigma_{i=1}^{m}[\alpha_i + \tau_i \cdot \|B_i\|] < 1$ implies that all roots of eqn. 4 lie in the open left plane of complex plane z, i.e. $\alpha_D := \sup\{\mathrm{Re}z : \det[\Delta(z)] = 0\} < 0$. This completes the proof in view of [1], theorem 9.3.5. □

We now present a delay-dependent criterion for the asymptotic stability of the system of eqn. 3.