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Simulation of Si multiple tunnel junctions

H.-O. Müller[a,*], D.A. Williams[a], H. Mizuta[a], Z.A.K. Durrani[b], A.C. Irvine[b], H. Ahmed[b]

[a]*Hitachi Cambridge Laboratory, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, UK*
[b]*Microelectronics Research Centre, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, UK*

Abstract

Single electron multiple tunnel junctions (MTJs) provide a useful means of achieving Coulomb blockade effects using silicon technology. A blocking dot model is developed for the simulation of these MTJs. Our simulation uses a single-electron simulator integrated into a SPICE-type conventional circuit simulator, thus allowing for the simulation of MTJ-based memory cells. © 1999 Elsevier Science B.V. All rights reserved.

Keywords: Coulomb blockade; Memory cell; Circuit simulation

Recently, operation of a Coulomb blockade-based memory cell with read-out transistor (gain cell) was demonstrated [1]. The Coulomb blockade element of this cell was a single electron multiple tunnel junction (MTJ, Fig. 1) which forms in doped silicon wires for appropriate values of the side gate voltage V_{sg}. It connects the word line of the memory cell to the memory node, which in turn is placed on the top of the gate oxide of a MOSFET (metal-oxide semiconductor field effect transistor). The charge state of the memory node holds the information and the MOSFET current tests this state. Thus, gain cell operation and non-destructive read out are achieved.

Qualitatively the behavior of the MTJ was understood during the first experiments on this system [2]: the MTJ consists of a system of nano-scale dots connecting both leads. The geometry of the system changes with the applied side gate voltage. For sufficiently negative V_{sg} the nano-dots are small, rare, and far apart and the MTJ is pinched off. In contrast, for sufficiently positive voltage the dots coalesce and conduction becomes ohmic. For memory operation the voltage is chosen between these two extremes [1].

For a fixed side gate voltage, the geometry of the dot system depends mainly on the stochastic dopant distribution. Therefore, the dot structure might be complicated, it might vary from sample to sample, and it might be hardly accessible numerically [3]. These difficulties can be avoided by employing a single-dot model, where the dot size depends on the side gate voltage. This approximation is able to produce Coulomb blockade and Coulomb oscillations, as observed in MTJs [2]. It shows the side gate influence as well. In this regard it is a very simple model satisfying both conditions.

Geometric considerations show that the nano-dot size is about 20–30 nm whereas the wire, which hosts the MTJ, is about 50 nm wide. Therefore, the

* Corresponding author. Tel: + 44-1223-442904; fax: + 44-1223-467942.

E-mail address: hom@phy.cam.ac.uk (H.-O. Müller)

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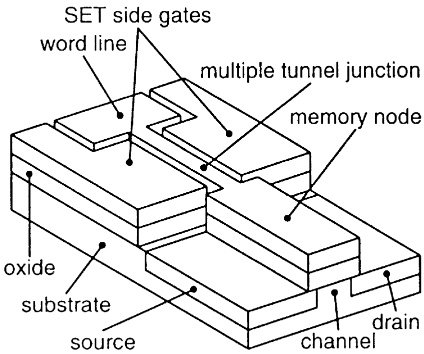

Fig. 1. The LSEM memory cell. The MTJ connects the word line to the memory node.

MTJ is in reality a rather one-dimensional chain of dots of different size. As the smallest dot in this chain produces the largest blockade voltage, the MTJ is essentially influenced by this one dot, the blocking dot of the whole MTJ. For our simulation the MTJ is therefore replaced by a double junction.

We determine the dot size as function of the side gate voltage by means of a phenomenological fit to experimental data. In Fig. 2 we plot the dot capacitance C_Σ as function of the side gate voltage V_{sg}. This capacitance can be obtained from the experimental observation of the Coulomb blockade, $C_\Sigma = e/(2\,V_b)$, and it can be calculated from the dot size [4]. Assuming a functional dependence of the dot size on the side gate voltage allows for a fit to the experiment. We use three test functions for this procedure: $r \propto V_{sg}$, $r \propto V_{sg}^{-1}$, and $r \propto \exp[V_{sg}]$. In the lower panel of Fig. 2 we plot the obtained dot radii. Since the fit yields the dot separation as well, we can determine the points of coalescence for the different functions. They are indicated by arrows.

While the fit itself produces reasonable values of C_Σ for all three of our test functions, the points of coalescence scatter considerably and only the exponential *ansatz* produces realistic results: the dot diameter varies from 15 to 30 nm while the center-to-center distance is about 22 nm. Coalescence is observed for $V_{sg} \approx -3.8$ V, which fits well to the experimental observation. We use this model for the remaining part of our study. The exponential dependence can be explained by the screened Coulomb interaction between electrons in the side gate and in the MTJ.

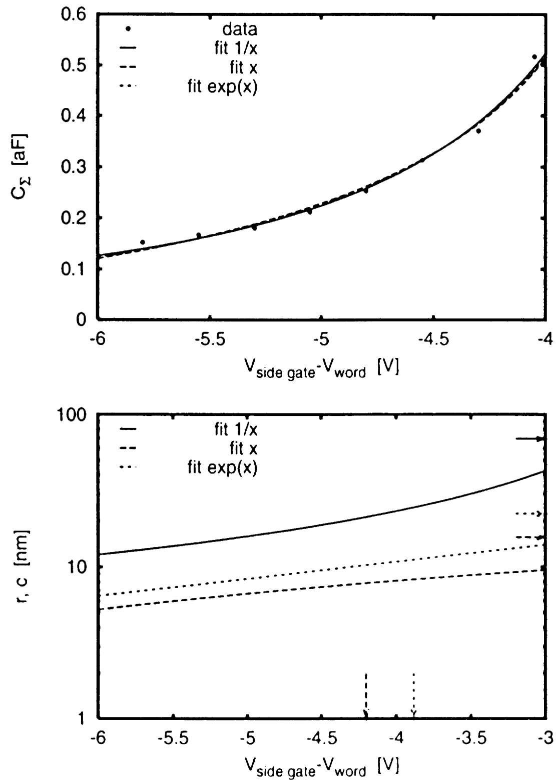

Fig. 2. Retrieving the parameters of the blocking dot from a fit to experimental data. Upper panel: C_Σ as function of V_{sg} as taken from the experiment (●), and the fit to three test functions. Lower panel: the dot radii as produced by these test functions. Arrows indicate the points of coalescence.

Given all electrical parameters of the MTJ system, the transported current is computed using standard techniques [5]. Due to the simplicity of our model the stationary solution of the orthodox master equation can be calculated directly and quickly produces accurate results (compared to the convoluted Monte-Carlo procedure).

Fig. 3 shows a contour plot of the MTJ current. Typical fingerprints of the charging effect are clearly observed, i.e. Coulomb blockade and Coulomb oscillations. They disappear for high side gate voltage in the coalescence regime. Specific to the blocking dot model is the side gate dependence of the Coulomb blockade. Note that due to effects of the stray capacitances the Coulomb oscillations resemble that of an asymmetric double junction [6].

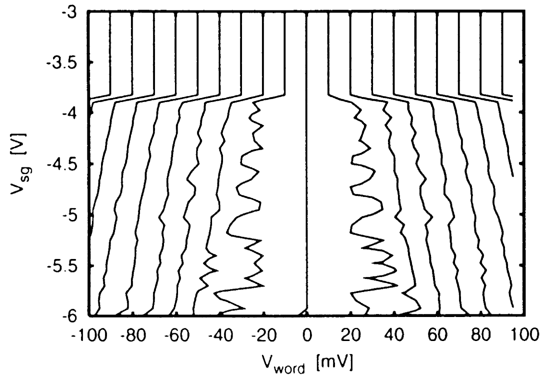

Fig. 3. Contour plot of the current through an MTJ. For large V_{sg} the MTJ is ohmic. The I–V characteristic shows asymmetric behavior. A change in the dot capacitance is observed.

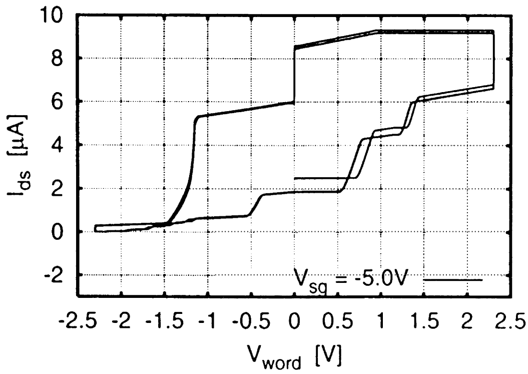

Fig. 4. Simulated hysteresis curve of a memory cell. V_{sg} is $-$ 5.0 V.

As mentioned above, an MTJ can be used in a memory cell. The cardinal difference to the case discussed before is the non-vanishing potential of the memory node, which alters the potential difference to the side gate, and thus the size of the blocking dot. Another problem, but outside the scope of this work, is the unified simulation of small-capacitance single electron elements in a classical circuit [7,8].

We plot a memory cell hysteresis curve in Fig. 4. Side gate voltage and MOSFET source-drain voltage are fixed to $-$ 5.0 and 4.0 V, respectively. The word line voltage V_w cycles between $\pm$ 2.3 V (four simulated cycles). In the plot, the resulting transistor current is plotted as a function of the applied word line voltage. Due to the charge storage on the memory node the transistor characteristic changes and hysteresis is observed. In turn, the different states of the memory node can be sensed via the transistor current.

The coupling of the memory node voltage to the device characteristics is a unique feature of this memory cell and invites more exploration. Other open questions include the effect of the tunnel resistance and the resulting difference between the memory charge states.

In conclusion, we have proposed a simple model for the simulation of an MTJ. The model features a size-variable single dot. Its electrical characteristics have been simulated and compared to that found in MTJs.

MTJs can be used in memory cells. In this case, feed-back occurs between the memory node voltage and the geometry of the MTJ, which determines the memory node voltage. Some simulation results have been shown and discussed.

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