# Design and Analysis of High-Speed Random Access Memory with Coulomb Blockade Charge Confinement

Kozo Katayama, Hiroshi Mizuta, *Member, IEEE*, Heinz-Olaf Müller, David Williams, *Member, IEEE*, and Kazuo Nakazato

***Abstract*— A silicon-based memory cell utilizing Coulomb blockade is analyzed for use as a high-speed RAM. Operation principles and design guidelines are given by simple analytical modeling and simulations. By performing transient waveform Monte Carlo simulations, high-speed write operation is demonstrated with a time shorter than 10 ns. The memory node voltage of less than 0.1 V is detected by a newly proposed split-gate cell structure with a minimum disturbance to/from nonselected cells, which indicates the compatibility of this structure with conventional field effect transistors.**

***Index Terms*— Cell design, Coulomb blockade, high-speed RAM, simulation, single electron.**

## I. Introduction

PRESENT memory architectures such as the dynamic random access memory (DRAM) are now approaching fundamental difficulties. One of the inherent problems in DRAM is the amount of charge stored in cell capacitors. The amount of stored charge must be maintained to ensure noise margins sufficient for sense amplifiers to detect the signal. This is a serious restriction on the further scaling down of DRAM cell sizes. Therefore, the gain cell structure realized in FLASH memories is a candidate to remedy the situation, along with the development of high dielectric capacitor materials. Nanocrystal memories proposed recently [1], [2] have a potential to realize small memory cells, where stored charge might be scaled down to a single electron. However, in these cells, charge is injected into floating nanocrystals through potential barriers such as gate oxides by standard (Fowler–Nordheim) tunneling processes, as in FLASH memories. Consequently, the write speed is rather slow in these memories compared to the present DRAM. In this paper we propose a new memory cell architecture called lateral single electron memory (L-SEM) which enables high-speed write operation comparable to DRAM. In this scheme, a tunnel junction array with small junction capacitances and relatively low tunnel resistances is used to inject and remove the charge stored in the memory node, instead of the tunnel oxide used in FLASH-type nanocrystal memories.

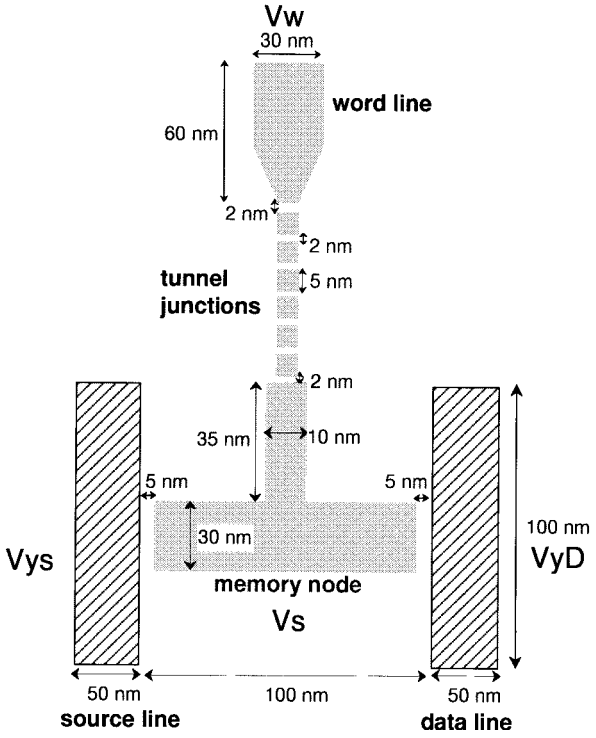



Fig. 1. L-SEM structure with a one-dimensional tunnel junction array and a memory node which acts as the gate of the sense MOSFET.

## II. Design and Operation Principles

In this paper, we consider the memory cell structure shown in Fig. 1, which is based on the recent experimental work [3]. An in-plane tunnel junction array [4] is integrated into the gate of a MOSFET, and the write operation is achieved by electrons tunneling through the junctions between the word electrode and the memory node. The stored data is maintained by the Coulomb blockade of the tunnel junctions and is sensed by applying a small voltage between the source and the drain electrode. The single electron switching operation of the tunnel junctions is not used in this scheme. As a result, the background charge effects which are serious in single-electron transistor operations are greatly alleviated [5]. An array of

Manuscript received July 23, 1998; revised April 22, 1999. This work was performed within the ESPRIT MEL-ARI project FASEM (Fabrication and Architecture of Single-Electron Memories). The review of this paper was arranged by Editor D. P. Verret.

K. Katayama was with Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Cambridge CB3 0HE, U.K. He is now with Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185, Japan.

H. Mizuta, H.-O. Müller, D. Williams, and K. Nakazato are with Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Cambridge CB3 0HE, U.K.

Publisher Item Identifier S 0018-9383(99)07210-X.

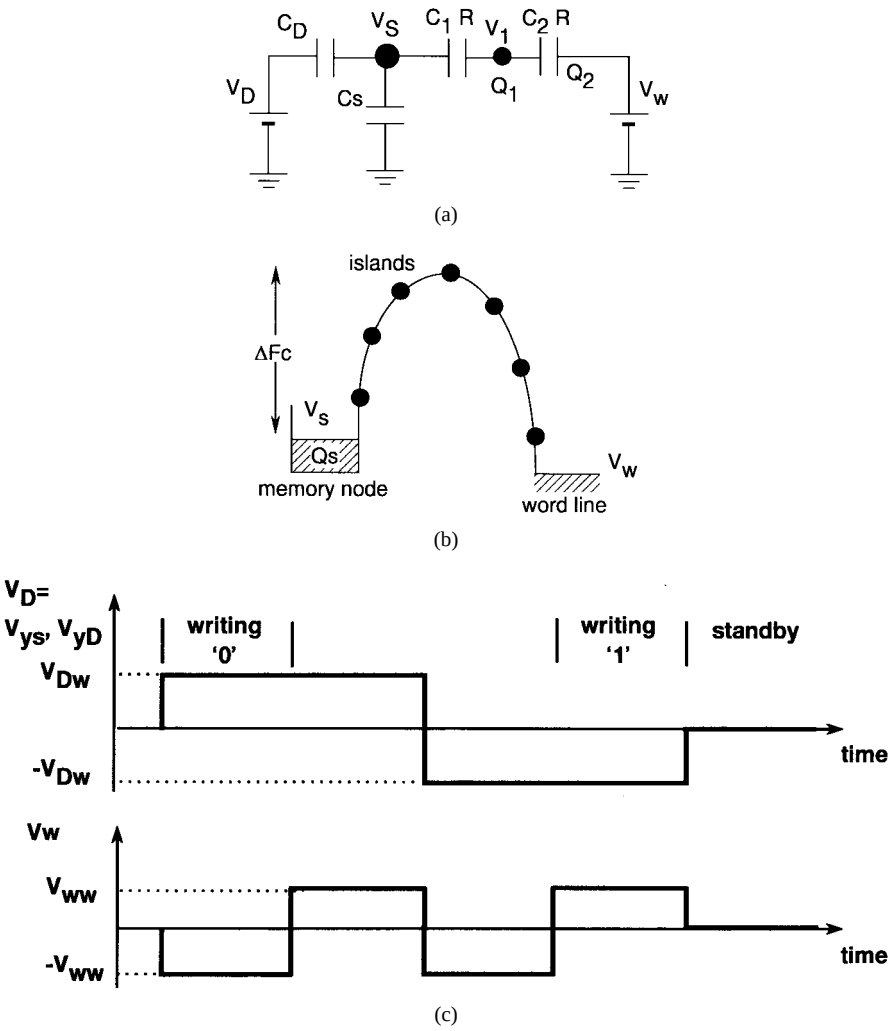



Fig. 2. (a) Simplified equivalent circuit for analytical modeling of the memory cell, (b) potential barrier due to Coulomb blockade, and (c) applied voltages in write operation and standby states.

tunnel junctions is effective in obtaining a higher Coulomb gap as well as in averaging out the background charge fluctuations.

The Coulomb gap $V_c$ of an infinitely long, uniform array is given as [6]

$$V_c = \frac{e}{C_g + \sqrt{C_g^2 + 4C_tC_g}} \tag{1}$$

where $C_t$ and $C_g$ are tunnel junction and stray capacitances and $e$ is an elementary charge. The number of junctions should be about $\sqrt{C_t/C_g}$ because $V_c$ approaches the value of (1) at the junction length $\sqrt{C_t/C_g}$. The Coulomb gap of disordered arrays due to the effect of background charge and other effects is discussed in [5], [7], and [8].

### *A. Write Operation*

To analyze the operation of the memory, a simplified equivalent circuit described in Fig. 2(a) is considered. Since the free energy of the system has a maximum value, as shown in Fig. 2(b), when the charge is placed at one of central islands, only this island is taken into account. We assume $C_1$ as the total serial capacitance between the island and the memory node and $C_2$ as that between the island and the word line. $C_s$ is the memory node capacitance which is realized by the gate of a MOSFET. The write operation sequence is described in Fig. 2(c). To write "0", positive $V_D = V_{ys} = V_{yD}$ is applied to the common source and data line of the selected column of the array to shift the memory node voltage, and at the same time, a negative word line voltage $V_w$ is applied to a selected row. In this way, a cell is selected out of the entire array. To write "1", the opposite polarity voltages are applied to the data and word line, which brings the "0" state outside the blockade region and causes a transition. The memory node voltage $V_s$ when $V_w$ and $V_D$ are applied is given as

$$\begin{aligned} V_s &= (C_TV_w + C_DV_D + Q_s)/C_\Sigma. \\ C_\Sigma &= C_T + C_D + C_s, C_T = C_1C_2/(C_1 + C_2). \end{aligned} \tag{2}$$

If $|V_w - V_s| > V_c$, the memory node is charged until $|V_w - V_s| = V_c$ is satisfied. Combined with (2), the word line voltage $V_{ww}$ and data line voltage $V_{Dw}$ required to charge the memory node to $Q_{s0}$ is obtained as

$$V_{ww} = \frac{C_\Sigma V_c - C_DV_{Dw} + |Q_{s0}|}{C_s + C_D}. \tag{3}$$

$|Q_{s0}|/C_\Sigma < V_c$ has to be satisfied to keep the data at the standby condition when $V_w$ and $V_D$ are kept at zero. To avoid data destruction in nonselected cells to which one of $V_{ww}$ and $V_{Dw}$ is applied during write cycles, the following conditions are required:

$$(2(C_s + C_D)V_{ww} + C_D V_{Dw})/C_\Sigma < 2V_c \tag{4}$$

$$((C_s + C_D)V_{ww} + 2C_D V_{Dw})/C_\Sigma < 2V_c. \tag{5}$$

When the write voltages are sufficiently high, the time required to charge up the memory node is simply given by the $CR$ time constant of the system

$$t_{THL} = R_T C_\Sigma \tag{6}$$

where $R_T$ is the total resistance of serial tunnel junctions.

### B. Retention Time

The retention time of the memory can be evaluated based on the orthodox theory of single electron tunneling [9]. The electrostatic energy of the system $F$ as a function of the memory node charge $Q_s$, the island charge $Q_1$, and the word line voltage $V_w$ is calculated based on the thermodynamics of electrostatic systems

$$dF(Q_s, Q_1, V_w) = V_s dQ_s + V_1 dQ_1 - Q_2 dV_w. \tag{7}$$

Solving charge conservation relations

$$\begin{aligned} C_s V_s + C_1(V_s - V_1) &= Q_s \\ C_1(V_1 - V_s) + C_2(V_1 - V_w) &= Q_1 \\ C_2(V_w - V_1) &= Q_2, \end{aligned}$$

we obtain $V_s, V_1$, and $Q_2$ as

$$\begin{aligned} V_s &= \frac{(C_1 + C_2)Q_s + C_1 Q_1 + C_1 C_2 V_w}{(C_1 + C_2)C_s + C_1 C_2} \\ V_1 &= \frac{C_1 Q_s + (C_1 + C_s)Q_1 + C_2 C_s V_w}{(C_1 + C_2)C_s + C_1 C_2} \\ Q_2 &= \frac{C_2(-C_1 Q_s - (C_1 + C_s)Q_1 + C_1 C_s V_w)}{(C_1 + C_2)C_s + C_1 C_2} \end{aligned}$$

where we assumed $V_D$ is fixed at zero and $C_D$ is included in $C_s$. Integrating (7) and calculating the difference between the final and the initial states of a single charge tunneling event, the barrier height $\Delta F_c$ is given as

$$\begin{aligned} \Delta F_c &= \min(F(Q_s - e, e, 0) \\ &\quad - F(Q_s, 0, 0), F(Q_s, -e, 0) - F(Q_s, 0, 0)) \\ &= \frac{eC_s}{C_{s1}}(V_c - Q_s/C_{s2}) \\ C_{s1}^{-1} &= \frac{\max(C_1, C_2)}{(C_1 + C_2)C_s + C_1 C_2} \\ C_{s2}^{-1} &= \frac{C_1 + C_2}{(C_1 + C_2)C_s + C_1 C_2} \end{aligned} \tag{8}$$

where the Coulomb gap $V_c$ is

$$V_c = \frac{e}{2C_s}\left(1 + \frac{C_s}{\max(C_1, C_2)}\right). \tag{9}$$

When $C_1, C_2 \ll C_s$, (9) is reduced to $V_c = e/2\max(C_1, C_2)$ which is independent of $C_s$. Thus, a memory cell with a large node capacitance does not deteriorate the Coulomb blockade characteristics.

The tunneling rate $1/\tau_c$ is expressed according to the orthodox theory of single electron tunneling as

$$\begin{aligned} 1/\tau_c &= \frac{\Delta F_c}{e^2 R} \Big/ \left(\exp\left(\frac{\Delta F_c}{k_B T}\right) - 1\right) \\ &\approx \frac{\Delta F_c}{e^2 R} \exp\left(-\frac{\Delta F_c}{k_B T}\right). \end{aligned} \tag{10}$$

We define the retention time of the memory $t_{1/2}$ as the half life time of the initial stored charge $Q_{s0}$, namely, $Q_s(t = t_{1/2}) = Q_{s0}/2$. Solving $dQ_s/dt = -e/\tau_c$, we obtain

$$\begin{aligned} Q_s(t) &\approx -a \ln\left\{\exp(-Q_{s0}/a) + \frac{\Delta F_c}{eaR}\exp(-C_{s2}V_c/a)t\right\} \\ a &= \frac{C_{s1}C_{s2}k_B T}{eC_s}. \end{aligned}$$

Hence

$$\begin{aligned} t_{1/2} &\approx \frac{2RC_{s2}C_{s1}^2 k_B T}{eC_s^2 V_c} \exp\left(\frac{eC_s}{C_{s1}k_B T}\left(V_c - \frac{3Q_{s0}}{4C_{s2}}\right)\right) \\ &\quad \cdot \sinh\left(\frac{eC_s Q_{s0}}{4C_{s1}C_{s2}k_B T}\right). \end{aligned} \tag{11}$$

When $C_1 = C_2 \ll C_s$, substituting $Q_{s0} = 4(\ln 2)C_s k_B T/e$ which maximizes (11), we finally obtain a simple formula for the retention time as a function of $V_c$

$$t_{1/2} \approx \frac{RC_s k_B T}{eV_c}\exp\left(\frac{eV_c}{2k_B T}\right) = \frac{RQ_{s0}}{4(\ln 2)V_c}\exp\left(\frac{eV_c}{2k_B T}\right). \tag{12}$$

## III. Simulation of Write and Read Operation

### A. Write Operation

To estimate the possible write-speed performance of the L-SEM, the structure shown in Fig. 1 was investigated including all the coupling constants between small islands and electrodes on a silicon substrate. Design parameters were chosen within the possible reach of present-day silicon nanowire formation technologies [10]. Detailed capacitance parameters between every conductor on the plane were determined by a two-dimensional (2-D) capacitance simulator, with which all the self- and cross-capacitances between the conductors are calculated under the assumption of negligible conductor thicknesses. Full memory write sequences were then simulated using a single-electron Monte Carlo simulator [5], [11] based on the orthodox theory of single electron tunneling without cotunneling effects. The simulation was done for a temperature of 4.2 K for a 5-nm-island memory cell with tunnel junction resistances of 1 MΩ, which is sufficiently larger than the quantum resistance $R_Q = h/4e^2$. If the full capacitance parameters are reduced to conform with the simplified circuit discussed in the previous section, memory node capacitance $C_s$ is ~32 aF, $C_D \sim 15$ aF, $C_t \sim 0.37$ aF, and $C_g \sim 1.9$ aF for this structure. The expected Coulomb gap is 40 mV from

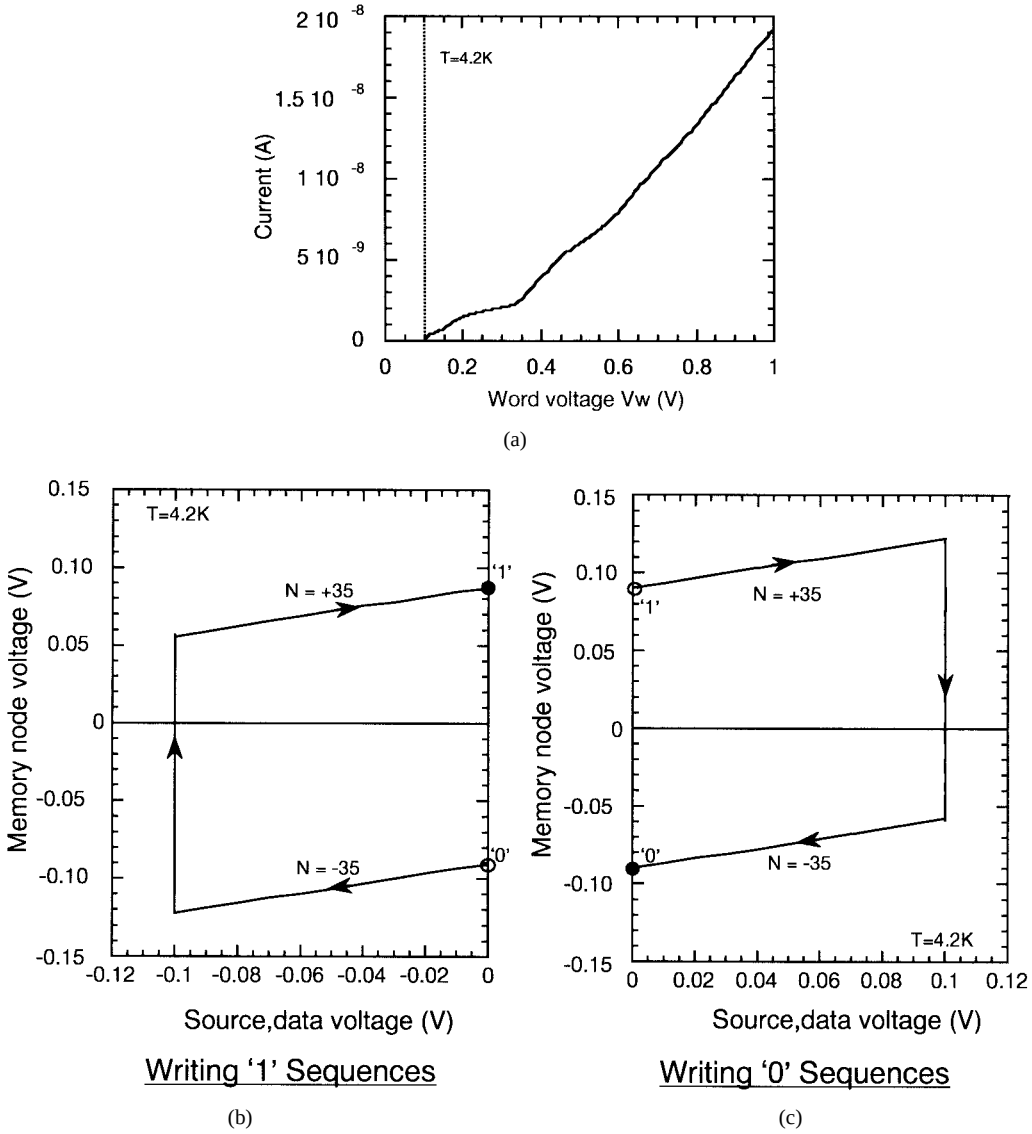


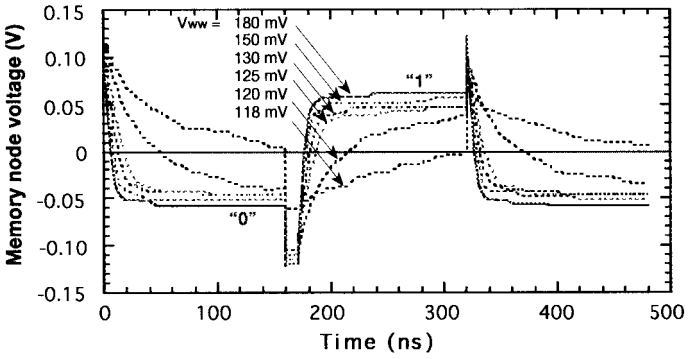

Fig. 3. (a) Simulated Coulomb blockade characteristics of a 1-D tunnel junction array with six $5 \times 5$ nm$^2$ islands in the geometry shown in Fig. 1. A Coulomb gap of 0.1 V is realized with this size of island. (b), (c) The hysteresis loop of the memory node voltage as a function of common source and data voltage $V_D$, obtained by a Monte Carlo simulation when the write sequence cycle in Fig. 2(c) with $V_{ww} = 180$ mV and $V_{Dw} = 100$ mV was executed. The upper and lower branches of the hysteresis correspond to $+35$e (the absence of 35 electrons) and $-35$e (the presence of 35 electrons) charge states, respectively.

(1), and $V_{Dw} \sim 100$ mV and $V_{ww} \sim 120$ mV are required to write the data.

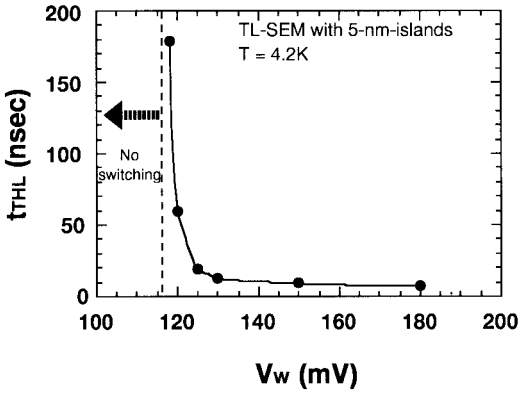
Fig. 3(a) shows the Coulomb blockade characteristics of the tunnel junction array obtained by a Monte Carlo simulation. Based on this obtained value of $V_c$ and the conditions (3), (4), and (5) $V_{Dw}$ and $V_{ww}$ were chosen to be 100 and 180 mV, respectively, and the write sequence operation was simulated. Fig. 3(b) shows the simulated node voltage hysteresis characteristics when the voltage sequence shown in Fig. 3(c) is applied. The upper branch of hysteresis corresponds to the state "1" where 35e charges are stored at the memory node and the lower branch to the state "0" with $-35$e charges. The temporal evolution of the memory node voltage during write cycles is shown in Fig. 4(a) for various word line voltages. The rise and fall time of the curves depends strongly on the word line voltage. The switching becomes faster with increasing $V_{ww}$ since a larger $V_{ww}$ results in a larger tunneling current through the tunnel junctions, leading to faster charging-up. In Fig. 4(b), the switching time $t_{THL}$ is plotted as a function of $V_{ww}$, where $t_{THL}$ is defined as the $1/e$ time of the curve. The switching occurs at a threshold voltage determined by (3) with $Q_{s0} = 0$ and then $t_{THL}$ decreases rapidly. It can be seen that $t_{THL}$ can be reduced to less than 10 ns for the present cell structure.

### *B. Read Operation*

Based on the concept of the L-SEM structure discussed so far, we designed a realistic memory cell on a silicon wafer including consideration of the read operation. The first problem to be considered for an SET-MOSFET hybrid structure, such as the L-SEM, is the operation voltage difference between SET and MOSFET. The node voltage is sensed by monitoring the current through the MOS channel induced under the memory node. Special care must be taken to read the data

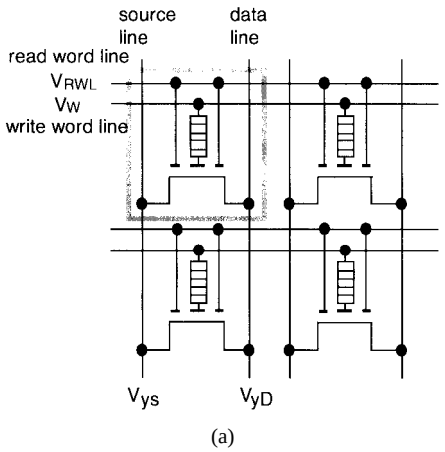



(a)

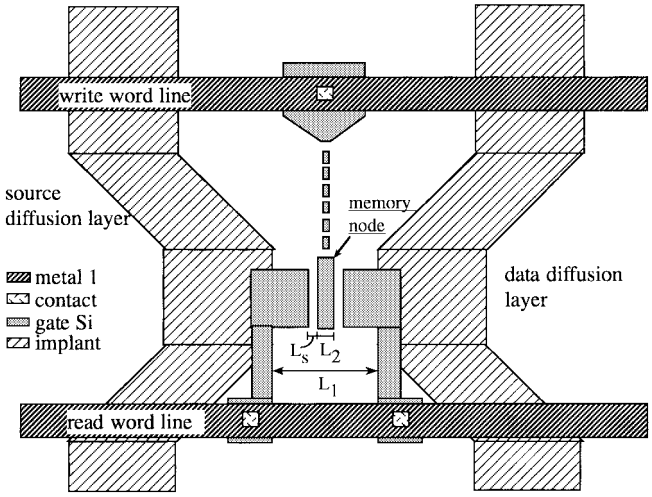



(b)

Fig. 4. (a) Transient memory node voltage simulated with various values of $V_{ww}$ for the L-SEM with 5 × 5-nm$^2$-island tunnel junctions at 4.2 K. (b) $V_{ww}$ dependence of rise/fall time $t_{THL}$. Fast switching is achieved between high and low levels with a switching time as short as 10 ns.




(a)



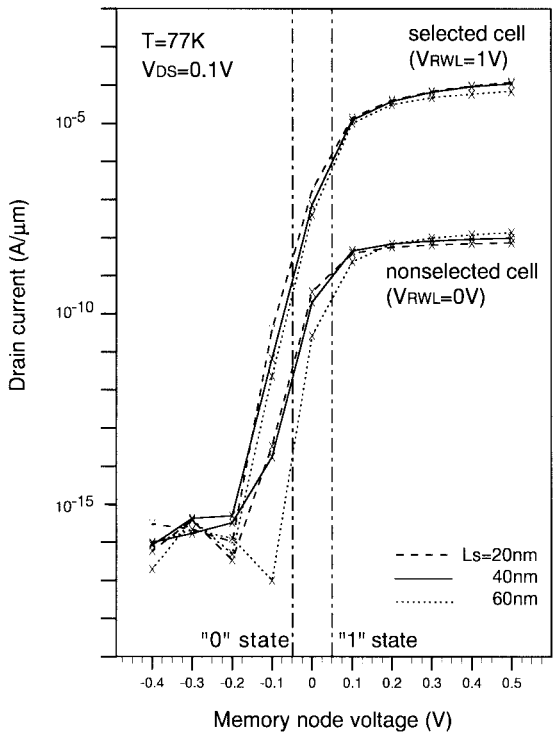

(b)

Fig. 5. (a) Equivalent circuit of a cell array for the split-gate memory node scheme. (b) A layout of the cell structure with split-gate MOSFET's. The original gate (length: $L_1$) is divided into three parts. The memory node gate (length: $L_2$) is separated from the two side gates with a spacing of $L_s$.

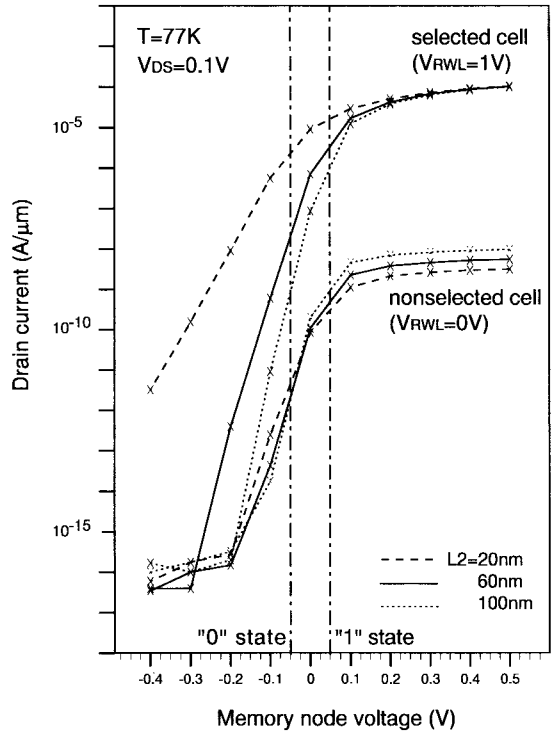
nondestructively in a selected cell in an array, because the Coulomb blockade voltage is low. The second problem is how to realize a small memory node size compatible with the small scale of tunnel junctions, because conventional MOSFET's have scaling limitations due to short channel effects. In order to reduce the memory node size, we propose a cell selection scheme shown in an equivalent cell array circuit [Fig. 5(a)], where a selected memory node is connected to the data line through MOSFET's driven by a separate read word line. A realistic cell layout for this structure is shown in Fig. 5(b). A diffusion layer is used for the source and data line to reduce the number of metal layers. The gate of the MOSFET is divided into three parts, the middle one of which is the memory node. The other two parts of the gate act as switch transistors to connect the memory node MOSFET to the data line. The threshold voltage of the memory node MOSFET is set between the charge states of "0" and "1". The size of the memory node can thus be made smaller than without the side gates (Fig. 1), because the short channel effect is relaxed by them. However, it should be noted that the smaller the node size is, the higher Coulomb gap is still required because $V_s$ is raised higher by the capacitive coupling with the read word line during read operations. The required Coulomb gap for nondestructive reading is given as $\sim V_{RWL}C_{RWS}/(C_s + C_{RWS})$, where $C_{RWS}$ is the capacitance between the side gates and the memory node.

The characteristics of this sense MOSFET were investigated by using a 2-D device simulator with the conventional drift-diffusion model. Simulated drain current characteristics of read MOSFET's for the split-gate structure are shown in Fig. 6. We assumed $V_{RWL} = 1$ V is applied to a selected word line, whereas a nonselected word line is kept at zero. Sufficient current modulation can be obtained by changing the memory node voltage. The drain current can flow as much as 1 $\mu$A/$\mu$m for a 50 mV node voltage. If we assume a 0.1 × 0.1 $\mu$m memory node size, about ten electrons are stored at the voltage. The change of the memory node voltage between −50 and 50 mV modulates the drain current by three orders of magnitude and the current difference between the selected and nonselected cell also amounts to three orders of magnitude. These signals will be sufficient to be amplified by standard MOS sense amplifiers even for a realistic large array size with 128 × 128 cells.

Fig. 6(b) shows the dependence of the $I$–$V$ characteristics on the memory node size $L_2$, which is changed from 20 to 100 nm. When the memory node size is as small as 20 nm, subthreshold leakage current is increased due to the short




(a)




(b)

Fig. 6. (a) Dependence of the $I-V$ characteristics of sense MOSFET's on the gap length $L_s$ of the split-gate. $L_s$ was changed between 20 and 60 nm. The memory node gate length $L_2$ was kept at 0.1 $\mu$m. (b) Dependence of the $I-V$ characteristics of sense MOSFET's on the memory node size $L_2$. $L_s$ was kept at 40 nm. Other relevant parameters in the simulation are: side gate length 0.36 $\mu$m, gate oxide thickness 10 nm, drain voltage 0.1 V, temperature 77 K. The doping profile of the MOSFET's was chosen so that the threshold voltage became $\sim$0 V, namely, n-type doping of $5 \times 10^{16}$ cm$^{-3}$ at the surface with the p-type substrate of $2 \times 10^{16}$ cm$^{-3}$.

channel effect because no doping profile optimization is done in this simulation. When a 20 $\times$ 20 nm memory node is realized, the stored charge in the memory node would be reduced to a few electrons.

## IV. Discussion

Our analyses carried out so far suggest that a write speed comparable with the present DRAM is achieved, with the possibility of combining a Coulomb blockade memory with conventional MOS transistors to read the data. The largest problem left to be investigated is the retention time. Assuming $Q_{s0} = 10e,\ R = 1\ \mathrm{M}\Omega,\ T = 77$ K, and $V_c = 0.1$ V, the formula (12) gives $t_{1/2} = 10$ ns, although at $T = 4.2$ K the lifetime is almost infinite. To obtain a retention time of 1 s comparable with DRAM's, a Coulomb gap of 0.36 V is required at $T = 77$ K and 1.5 V at $T = 300$ K. This means that rather high voltage operation is required for such an atomic scale device.

From the cell layout point of view, a lot of optimization of the structure is required. The lateral structure proposed here has the apparent demerit of a large cell size. At present, there is no well-developed silicon-based technology to fabricate vertical tunnel junction layers with sufficiently small dimensions enough to exhibit the charging effect. A vertical tunnel junction fabricated, for example, by nitridation of silicon [12] might be available in realistic implementations.

In conclusion, we have shown design guidelines for a random access memory cell where data is maintained by Coulomb blockade, and which is compatible with conventional MOS transistors. With relatively low tunnel resistance junctions for which cotunneling can still be neglected, faster operation than present day DRAM is possible. However, compatibility between faster operation and longer retention time at a room temperature still remains to be solved.

## Acknowledgment

The authors would like to thank Dr. K. Ito for stimulating discussion about the problems of conventional memories and S. Biesemans for critical comments on the L-SEM cell structure and operation.

## References

[1] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Room-temperature single-electron memory," *IEEE Trans. Electron Devices*, vol. 41, pp. 1628–1638, 1994.

[2] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, and E. F. Crabeé, "A silicon nanocrystals based memory," *Appl. Phys. Lett.*, vol. 68, pp. 1377–1379, 1996.

[3] Z. A. K. Durrani, A. C. Irvine, H. Ahmed, and K. Nakazato, "A memory cell with single-electron and metal-oxide-semiconductor transistor integration," *Appl. Phys. Lett.*, vol. 74, pp. 1293–1295, 1999.

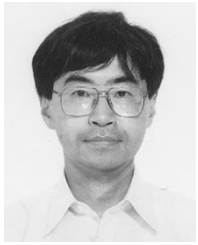
[4] K. Nakazato, R. Blaikie, and H. Ahmed, "Single-electron memory," *J. Appl. Phys.*, vol. 75, pp. 5123–5134, 1994.

[5] H.-O. Müller, K. Katayama, and H. Mizuta, "Effects of disorder on the blockade voltage of two-dimensional quantum dot arrays," *J. Appl. Phys.*, vol. 84, pp. 5603–5609, 1998.

[6] N. S. Bakhvalov, G. S. Kazacha, K. K. Likharev, and S. I. Serdyukova, "Single-electron solitons in one-dimensional tunnel structures," *Sov. Phys.—JETP*, vol. 68, pp. 581–587, 1989.

[7] A. A. Middleton and N. S. Wingreen, "Collective transport in arrays of small metallic dots," *Phys. Rev. Lett.*, vol. 71, pp. 3198–3201, 1993.

[8] J. A. Melsen, U. Hanke, H.-O. Müller, and K.-A. Chao, "Coulomb blockade threshold in inhomogeneous one-dimensional arrays of tunnel junctions," *Phys. Rev. B*, vol. 55, pp. 10638–10642, 1997.
[9] P. D. Dresselhouse, L. Ji, S. Han, J. E. Lukens, and K. K. Likharev, "Measurement of single electron lifetimes in a multijunction trap," *Phys. Rev. Lett.*, vol. 72, pp. 3226–3229, 1994.
[10] R. A. Smith and H. Ahmed, "Gate controlled Coulomb blockade effects in the conduction of a silicon quantum wire," *J. Appl. Phys.*, vol. 81, pp. 2699–2703, 1997.
[11] K. Nakazato and J. White, "Single-electron switch for phase-locked single-electron logic devices," in *IEDM Tech. Dig.*, 1992, pp. 487-490.
[12] H. Fukuda, J. L. Hoyt, M. A. MaCord, and R. W. F. Pease, "Fabrication of silicon nanopillars containing polycrystalline silicon/insulator multilayer structures," *Appl. Phys. Lett.*, vol. 70, pp. 333–335, 1997.



**Kozo Katayama** was born in Shizuoka, Japan, on December 10, 1957. He received the B.S., M.S., and Ph.D. degrees in electronic engineering, from the University of Tokyo, Tokyo, Japan, in 1980, 1982, and 1985, respectively.

He joined the Central Research Laboratory, Hitachi Ltd., Tokyo, in 1985. Since that time he has been engaged in the research of hot electron transport modeling in Si MOSFET's and low temperature physics such as macroscopic quantum tunneling in dissipative environment. During the period from 1995 to 1997, he worked for a 64-Mbit DRAM design project at Device Development Center, Hitachi Ltd. He stayed at Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Cambridge, U.K., from 1997 to 1998.

**Hiroshi Mizuta** (M'91) was born in Kochi, Japan, in 1961. He received the B.S. and M.S. degrees in physics and the Ph.D. degree in electrical engineering from Osaka University, Osaka, Japan, in 1983, 1985, and 1993, respectively.

He joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, in 1985 and has been engaged in research on numerical simulation of heterojunction devices as well as the study of resonant tunnelling devices. From 1989 to 1991, he has worked on quantum transport simulation, and also since 1997 he has been working on single-electron devices and other quantum devices at the Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Cambridge, U.K.

Dr. Mizuta is a member of the Physical Society of Japan, the Japan Society of Applied Physics, the Institute of Physics, and the IEEE Electron Devices Society.

**Heinz-Olaf Müller** received the diploma and Ph.D. degrees in physics from the Friedrich Schiller University, Jena, Germany, in 1990 and 1994, respectively.

He was awarded a post-doctoral fellowship with the Norwegian University of Science and Technology (NTNU), Trondheim, Norway, by the German Academic Exchange Council (DAAD) from 1995 to 1996. After a period with Lund University, Lund, Sweden, he joined Hitachi Cambridge Laboratory, Cambridge, U.K., in 1997. He is currently involved in the design and simulation of single-electron memory cells within the EU-funded FASEM project (fabrication and architecture of single-electron memory). He is also studying leakage mechanisms in poly-Si thin-film transistors.

**David Williams** (M'89) received the Ph.D. in physics from Cambridge University, Cambridge, U.K., in 1987.

He joined the Hitachi Cambridge Laboratory in 1989 and has worked on the physics and technology of nanostructures, including microscopy and electron transport measurements of devices made from bulk silicon, silicon-on-insulator, and III–V materials. Currently, he is working on single-electron memory structures and devices for quantum information processing.

**Kazuo Nakazato** was born in Tochigi, Japan, in 1952. He received the B.S., M.S., and Ph.D. degrees in physics from the University of Tokyo, Tokyo, Japan, in 1975, 1977, and 1980.

In 1981, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, working on high-speed silicon self-aligned bipolar devices which were adopted in main frame computer Hitachi M-880/420. In 1989, he moved to Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Cambridge, U.K., as Laboratory Manager and Senior Researcher, working on experimental and theoretical study of quantum electron transport in nanometer structures. Since 1997, he has been a Chief Researcher of Hitachi Cambridge Laboratory. His main concerns are single-electron and small electron-number devices.

Dr. Nakazato was granted a fellow of the Japanese Society for the Promotion of Science in 1980.