Coulomb blockade in silicon nano-pillars

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We have investigated the current–voltage characteristics of nano-pillars of polycrystalline silicon with two 2–3 nm thick silicon nitride tunnel barriers. Pillars with diameters between 45 and 100 nm showed a Coulomb blockade region and Coulomb staircase at 4.2 K. © *1999 American Institute of Physics.* [S0003-6951(99)01515-6]

Investigations of electron transport in nano-pillars in GaAs/GaAlAs heterostructures with well-defined barriers have shown Coulomb blockade oscillations as individual electrons are added to a quantum dot.[1] Similar structures in silicon are attractive because they are compact, have high, well-defined barrier heights, and are compatible with silicon technology. They also have advantages over lateral structures in disordered materials which show Coulomb blockade but do not always give a well-defined and reproducible number of islands and also over patterned nano-structures produced by lithography which present considerable fabrication challenges to obtain reproducible geometries and barrier heights. Fukuda *et al.*[2] demonstrated that ultrathin Si_3N_4 barriers can be formed in silicon pillars. We have fabricated such pillars using a silicon and silicon nitride layer structure and we present electrical characteristics of these pillars.

Figure 1(a) shows a schematic of the device structure. The polycrystalline silicon (polysilicon) was grown by low pressure chemical vapor deposition and phosphorous doped to $10^{19}\,cm^{-3}$ throughout. The wafer was heated to 900 °C in ammonia to produce a self-limiting 2 nm thick silicon nitride layer without breaking the vacuum. After further polysilicon growth a second nitride layer was grown and finally, the layers were completed with a polysilicon layer.

The pillars are defined using high resolution electron beam lithography in poly(methylmethacrylate) resist followed by gold evaporation and lift off to form the top contact. Reactive ion etching using a combination of $SiCl_4$ and CF_4 was used to provide a highly anisotropic etch which formed pillars with almost vertical side walls. A scanning electron micrograph of a pillar, showing the polysilicon and silicon nitride layers, is shown in Fig. 1(b). Planarization of the pillars was performed by spin coating and curing a polyimide film and etching back to the pillar tops so that electrical contacts can be made to the gold dot on top of the pillar.

Pillars with diameters between 45 and 100 nm were tested. Zero current regions in the range 5 to 25 mV have been recorded. The current–voltage ($I-V$) characteristics of most pillars show a staircase and are not symmetrical at 4.2 K. The $I-V$ characteristics for the devices with zero current regions larger than about 20 mV also showed slight conductance oscillations at 77 K. Negative differential conductance (NDC) on the first current step was observed for some pillars. Typical results for 50, 65, and 75 nm diameter pillars are included here.

The $I-V$ characteristics and differential conductance at 4.2 K for a 50 nm diameter pillar are shown in Fig. 2. A zero current region can be seen around zero source-drain voltage extending to ±6 mV. At higher voltages there is clear evidence of conductance oscillations giving a current plateau at ±14 mV and less clear second plateau around ±25 mV.

Figure 3 shows the source-drain current and differential conductance characteristics at 4.2 K for a larger 75 nm diameter pillar. For this device there is a less clear zero current region than for the 50 nm diameter pillar but five clear differential conductance minima (current plateaux) can be seen at positive values of applied voltage with the first at about 17 mV and there are three less clear conductance oscillations for negative applied voltages.

The 75 nm diameter device was tested again after drawing a current of 250 pA through the device. Figure 4 shows the same device before and after a 150 mV bias had been applied. After the bias had been applied a clear zero current region extending to ±12 mV is seen and the current staircase shifted. The first differential conductance minimum is now

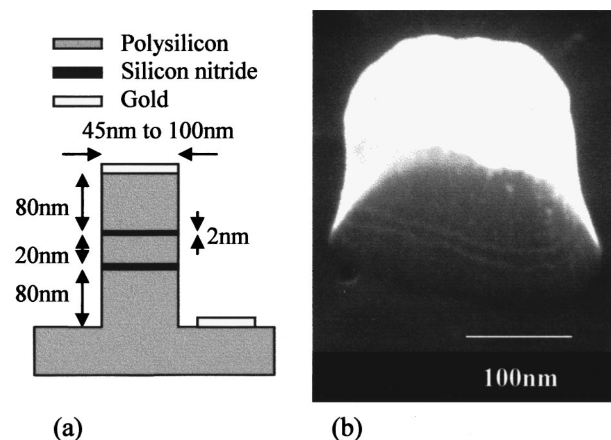

FIG. 1. (a) A schematic of the device structure. (b) A pillar, larger than those measured here, showing the two silicon nitride layers.

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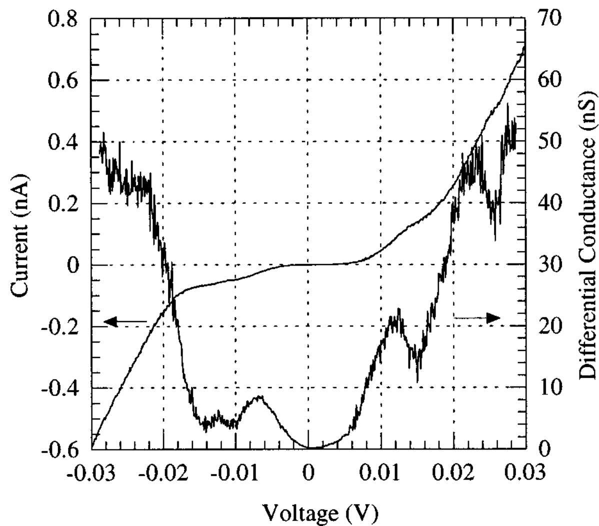

FIG. 2. The $I-V$ and differential conductance characteristics of a 50 nm diameter pillar at 4.2 K.

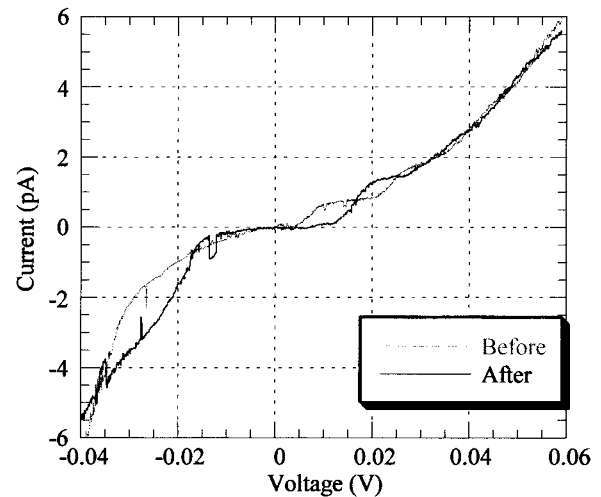

FIG. 4. The $I-V$ characteristic of the 75 nm diameter pillar before and after a source-drain voltage of 150 mV was applied, drawing a current of 250 pA through the device.

around +24 mV, but the separation between the steps is similar to that before the stress bias was applied. The changes remained for a few hours and disappeared overnight, reappearing when 150 mV was applied again the next day. Slight conductance oscillations were seen at 77 K for this device, but the conductance did not go to zero near 0 V.

The $I-V$ characteristics and differential conductance at 4.2 K for a 65 nm diameter pillar are shown in Fig. 5. The low conductance region is about 6 mV wide and differential conductance minima can be seen for positive and negative values of applied voltage. Negative differential conductance is seen around +14 mV.

The electrical results are consistent with the theory of Coulomb blockade.[3,4] The zero current around 0 V bias is clearly seen. Our device is expected to have different barrier resistances and asymmetry in the barriers leads to the appearance of a Coulomb staircase and accounts for the different characteristics in forward and reverse bias. From Fig. 2, we can see that the separation between adjacent steps of about 11 mV is equal to the Coulomb gap (to within the measurement errors). This is as predicted for the case of near zero offset charge on the island. The step separation gives a calculated value for the junction capacitance of 7 aF which is similar to the value of the junction capacitance obtained by treating the silicon nitride layer as the dielectric of a parallel plate capacitor.

For the 75 nm device the separation between current steps is approximately constant at 15 mV for the first four steps. At higher currents the steps are less distinct and so are harder to pinpoint accurately. The estimated junction capacitance of 5 aF is similar to that for the 50 nm pillar.

The observation of only slight conductance oscillations at 77 K compared with those at 4.2 K is also consistent with the Coulomb blockade effect as an explanation for our results since the thermal energy of 7 meV at 77 K is approaching the island charging energy of 15 meV so the oscillations are almost smeared out by thermal effects.

The behavior shown in Fig. 4 can be explained by the excess voltage bias causing one or more traps in an interface near to the island to be filled which alters the offset charge in

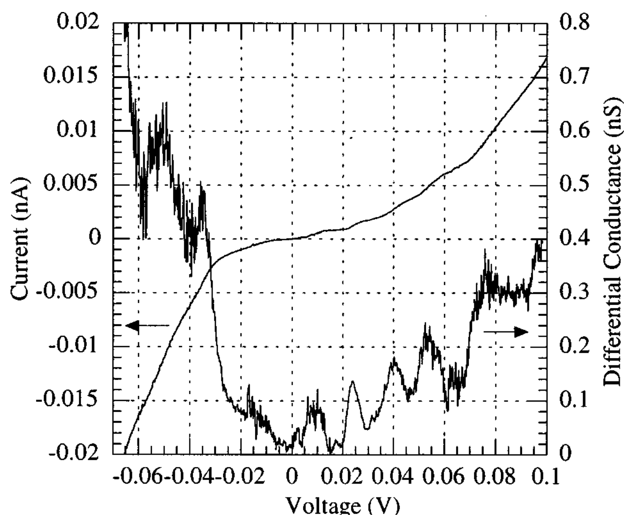

FIG. 3. The $I-V$ and differential conductance characteristics of a 75 nm diameter pillar at 4.2 K.

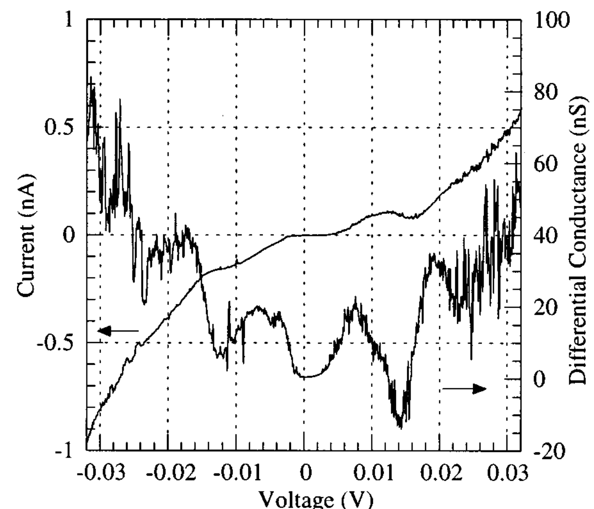

FIG. 5. The $I-V$ and differential conductance characteristics of a 65 nm diameter pillar at 4.2 K.

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the vicinity of the island and causes the staircase to be shifted. The separation between the current steps remains the same, while the Coulomb gap is altered due to the changed offset charge. After the charge has been trapped, the island is near to the zero net offset charge state since the Coulomb gap is nearly twice the separation between current steps. This is similar to the effect that a gate would have in a three terminal device. This behavior was only observed in one pillar but is included here as it lends weight to the Coulomb blockade explanation.

The NDC shown in Fig. 5 is thought to be due to resonant tunnelling of electrons. When the conduction band edge of the drain lines up with the first available electron state on the island, electrons can tunnel from the drain onto the island. At a slightly higher voltage, the resonance condition is no longer satisfied and the current is reduced leading to an NDC characteristic. A low peak to valley ratio is seen because of the various disorder effects in our system. Similar effects have been observed in lateral disordered silicon structures.[5,6]

Transport in polysilicon nanowires has shown nonlinear effects because of potential barriers at the grain boundaries which can act as tunnel barriers at low temperatures.[7,8] However, our pillars have a cross-sectional area which is many times greater than in these devices and many parallel conduction paths exist through the polysilicon. The pillars measured here are likely to be wide and short enough that strong potential barriers at some grain boundaries are shorted out by low resistance pathways through others. Measurements on single barrier devices have shown some Coulomb blockade like effects, but these were less pronounced than in the two barrier devices. Devices were measured at various temperatures and a plot of log (I) vs $1/T$ (K) showed that the blockade effect was stronger for the two barrier devices.

The results are shown for a single island, double barrier device but the layer structure can be extended to increase the number of islands, making the fabrication of vertical multiple-tunnel junctions possible. The operating temperatures can be raised by reducing the polysilicon thickness between two silicon nitride tunnel barriers.

In conclusion, we have shown evidence for Coulomb blockade in vertical polysilicon structures with a single island formed by two silicon nitride barriers. A memory effect thought to be due to charging in the vicinity of the island has also been observed in one sample.

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