Theoretical study of tunneling current in the access region of various heterojunction field-effect transistor structures

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The source resistance of a heterojunction field-effect transistor (HFET), whose reduction is mandatory for high-performance devices, consists of an ohmic contact resistance and an access resistance. The access region is located between the geometrical source and the geometrical source side of the gate contact. By means of a quantum-mechanical modeling program, the effect of changes in layer structure in the access region of a HFET is studied. A new heterojunction structure using a Si planar doped layer is designed to improve the linearity and reduce the access resistance by more than ten times for a specific transistor layout. Thanks to the higher sensitivity of the modeling program to structural information, the contribution of the tunneling current and the change of equilibrium as a function of temperature is investigated. © *1996 American Institute of Physics.* [S0021-8979(96)00307-6]

I. INTRODUCTION

In recent years, heterojunction field-effect transistors (HFETs) with ever increasing performances have been fabricated thanks to improvements in layer structure, layer growth, use of planar or delta-doped layers, and reduction of the source resistance.[1] The reduction of the source resistance is mandatory for high-performance HFETs as this resistance deteriorates the extrinsic transconductance, the maximum oscillation frequency, and minimum noise figure.[2] The source resistance can be commonly divided into two parts. The first part is the contact resistance which carriers experience when they flow from the contacting metal to the semiconductor. The second contribution results from carriers flowing from the ohmic contact region to the source side of the two-dimensional electron gas (2DEG) channel. This second resistance is the access resistance. Recent work has been mainly directed to the improvement of the ohmic contacts and the reduction of the access resistance by source-gate spacing reduction.[3,4]

The reduction of source-gate spacing is considered to be the most difficult and least reproducible step for high-yield device processing. The conditions for source-gate spacing reduction can however be relaxed by reducing the resistance of the access region. In this article a new structure is proposed which leads to a reduction of the access resistance due to enhanced tunneling and increased current density in various parts of the heterostructure.

A quantum-mechanical modeling program[5,6] has been used to compare the resistance value and linearity of the current–voltage characteristics with those of several other heterostructures achieving access resistance reduction. To obtain a quantitative description of the contribution of the tunneling current on one side and the thermionic/diffusion current on the other side, the current transport is analyzed as a function of temperature. Moreover, conclusions are drawn concerning the stability of the structure and its relative independence from external forces.

II. MODELED STRUCTURES DESIGN

The access resistance in a HFET structure consists in a first approximation of three parallel conduction paths as seen in Fig. 1. These three paths in a standard GaAs/AlGaAs/InGaAs source contact structure are the highly doped GaAs top layer, the undepleted AlGaAs electron supply layer, and the 2DEG channel. Under the geometric contact at the source we consider these three paths to be shorted. However, at a certain distance from this contact the voltage in the 2DEG channel will rise due to the resistance along the channel and perpendicular to the channel which is mainly determined by tunneling and thermionic emission over the heterojunction diodes.

For optimized structures, however, very little can be done about the resistance of the 2DEG channel, which is optimized toward highest electron density and so to lowest resistance. Although when the resistance across the vertical heterojunction diode is negligible, the total resistance can be reduced by reducing the top-layer resistance. Reduction of the top-layer resistance by replacing GaAs by $In_yGa_{1-y}As$ has been described by Kuroda *et al.*,[7] and by inserting an $In_yGa_{1-y}As$ quantum well between the electron supply layer and the top layer it has been described in former work.[2] These two techniques, however, do not take into account the increase in barrier height of the electron supply layer at the interface with the top layer, due to the larger heterojunction dipole which is created. As the vertical heterojunction diode resistance then becomes significant, the improvement obtained by these two techniques remains marginal.

Reduction of the vertical resistance has been obtained by placing a planar doped Si layer in the electron supply material or at the edge with the top layer material. These heterostructures require a more complex processing because the electron supply layer containing the planar doped Si layer

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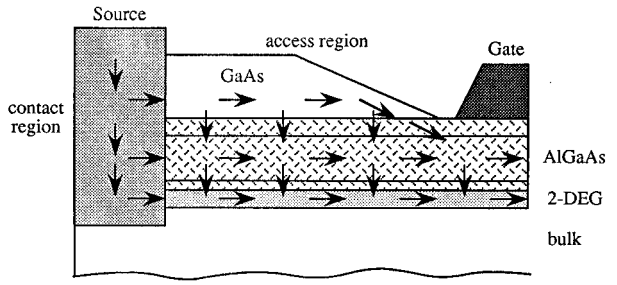

FIG. 1. Definition of the access region and the three parallel conducting paths which contribute to the access resistance in the HFET layer structure.

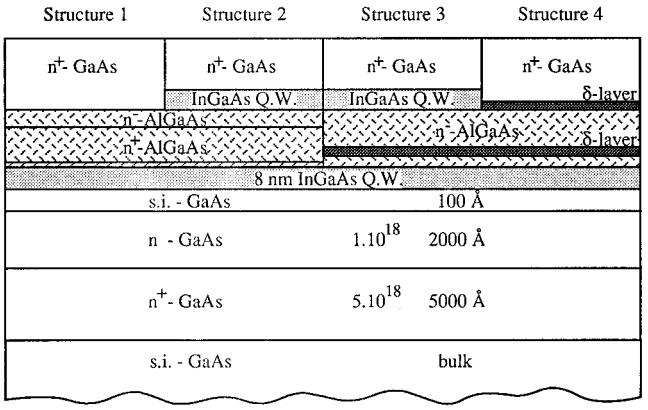

FIG. 2. Schematic layout of the HFET layer structure.

has to be partly removed during the gate etch in order to obtain high-quality Schottky diodes. The new heterostructure, presented here with a single Si planar layer in the top layer, combines the reduction of top layer resistance and of vertical heterojunction diode resistance. To obtain this structure the Si planar doped layer has to be grown in the same material as the top layer at a distance d, not farther from the electron supply layer than given by

$$0<d=\frac{nd}{5\times10^{18}\ \mathrm{cm}^{-3}}\leqslant 30\ \ \mathrm{nm},$$

with nd the total integrated doping of the Si planar doped layer.

Two fundamental heterostructures chosen from previous research[2] are the following. The uniformly doped heterostructure consists of a 500 nm n^+-GaAs layer (Si, 5×10^{18} at. cm^{-3}), a 200 nm n-GaAs layer (Si, 1×10^{18} at. cm^{-3}), a 10 nm semi-intrinsic (s.i.)-GaAs layer followed by an 8 nm s.i.-$In_{0.25}Ga_{0.75}As$ quantum well, a 2 nm s.i.-$Al_{0.25}Ga_{0.75}As$ spacer layer, a 25 nm n^+-$Al_{0.25}Ga_{0.75}As$ electron supply layer (Si, 3×10^{18} at. cm^{-3}), 10 nm n^--$Al_{0.25}Ga_{0.75}As$ layer (Si, 5×10^{17} at. cm^{-3}), and finally a 100 nm n^+-GaAs top layer (Si, 5×10^{18} at. cm^{-3}). The semi-intrinsic layers are stimulated with a 10^6 at. cm^{-3} Si doping.

The delta-doped heterostructure consists of a 500 nm n^+-GaAs layer (Si, 5×10^{18} at. cm^{-3}), a 200 nm n-GaAs layer (Si, 1×10^{18} at. cm^{-3}), a 10 nm s.i.-GaAs layer followed by an 8 nm s.i.-$In_{0.25}Ga_{0.75}As$ quantum well, a 5 nm s.i.-$Al_{0.25}Ga_{0.75}As$ spacer layer, a Si delta-doped layer with density 7×10^{12} at. cm^{-2}, a 32 nm n^--$Al_{0.25}Ga_{0.75}As$ layer (Si, 5×10^{17} at. cm^{-3}), and finally a 100 nm n^+-GaAs top layer (Si, 5×10^{18} at. cm^{-3}). The delta-doped Si layer is described as a layer with the same characteristics as the surrounding layers and the doping density is considered to be spread over 5 nm length.

To study the influence of an $In_yGa_{1-y}As$ top quantum well and the delta-doped layers, the following structures, schematically drawn in Fig. 2, are considered: The first structure is the uniformly doped heterostructure as described above; the second structure has a uniformly doped electron supply layer, as does the first structure, but the top layer contains a 5 nm n^+-$In_{0.25}Ga_{0.75}$ as top quantum well (Si, 5×10^{18} at. cm^{-3}) at the edge with the 10 nm n^--$Al_{0.25}Ga_{0.75}As$ layer; the third structure is the delta-doped heterostructure as described above, but the top layer contains a 5 nm n^+-$In_{0.25}Ga_{0.75}As$ top quantum well (Si, 5×10^{18} at. cm^{-3}) at the edge with the 32 nm n^--$Al_{0.25}Ga_{0.75}As$ layer; the fourth structure is the delta-doped heterostructure, but the top layer contains a delta-doped Si layer with density 7×10^{12} at. cm^{-2} at 2.5 nm from the edge with the 32 nm n^--$Al_{0.25}Ga_{0.75}As$ layer.

III. COMPUTER SIMULATION RESULTS

Using the drift-diffusion and quantum-mechanical modeling programs described in previous work,[2,5,6] the band structure, carrier density, and resistance of heterostructure diodes are analyzed.

To reduce the access resistance, a new structure, described as structure 4, is designed, based on the addition of a Si planar doped layer in the cap material, in front of the GaAs/AlGaAs top heterojunction. The vertical and horizontal resistance are reduced due to the vanishing of the top heterojunction barrier and due to the higher carrier density in the planar doped layer, respectively. The band diagram of the new heterostructure is obtained by combining the band diagram of a conventional delta-doped heterostructure with the one of a single Si planar layer as shown in Fig. 3(a).

Due to this combination principle, based on the linearity of the Poisson equation towards charge, the location as well as the density of the planar doped layer can be optimized for maximum performance. In Fig. 3(b) it is shown that the position of the Si planar layer can be changed with respect to the AlGaAs/GaAs heterojunction. It is not mandatory to have the planar layer near to the heterojunction to remove the heterojunction barrier. The design window for the location of planar layer, as described previously, is available by adapting the planar layer density. In Fig. 3(c) the carrier density in the structure is shown for the drift-diffusion and quantum-mechanical model simulation. The strong decrease of the carrier density in the AlGaAs/InGaAs heterojunction barrier, noticed in the drift-diffusion result, is not seen in the quantum-mechanical result as tunneling through this thin barrier is taken into account. The effect of resistance lowering by removal of the top heterojunction barrier can only be simulated using the quantum-mechanical modeling program.

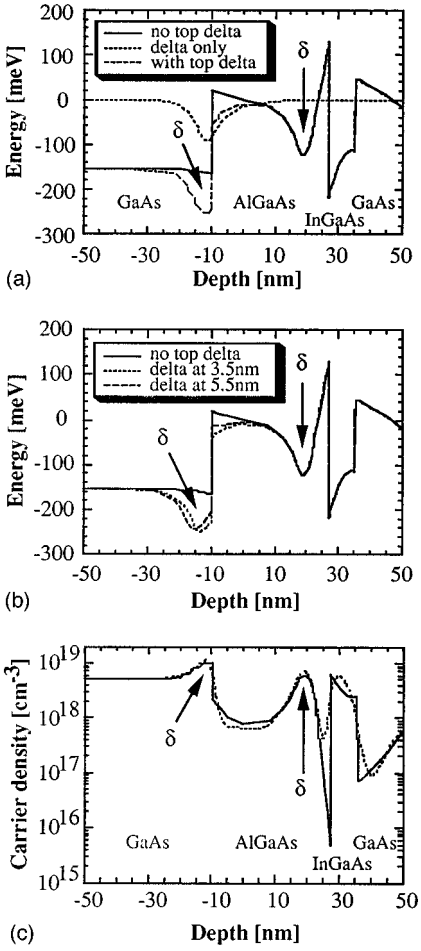

FIG. 3. (a) Combination of a Si planar doped layer (dotted line) with a conventional delta-doped HFET structure (solid line). The resulting structure is shown by the dashed line. (b) Band diagram comparison between the conventional delta-doped HFET and the structures with additional Si planar doped layer at 3.5 and 5.5 nm of the heterojunction. (c) Carrier density calculated by the drift-diffusion model (solid line) and the quantum-mechanical model (dotted line).

When using the drift-diffusion model the height of the AlGaAs/InGaAs barrier dominates the transport characteristics through the thermionic current equation.

The possibility of placing the Si planar doped layer in the top layer material is crucial for the practical realization of the HFET, which requires a high-quality Schottky diode for the gate. In this new structure a high-quality Schottky diode is obtained by the complete removal of the planar doped layer, together with the cap layer under the gate under standard etching conditions. This new structure can therefore also be used in selective etching processes for HFETs as the barrier material has a different composition than the cap layer material which contains the planar doped layer. The use of a planar doped electron supply layer improves the vertical current even more. Therefore, it is believed that the HFET structure with double planar doping is a good candidate for a minimum access resistance heterostructure.

Using the modified quantum-mechanical modeling program,[2] the dependency of resistance as a function of applied bias has been studied for a uniformly doped HFET structure and the newly presented structure with planar

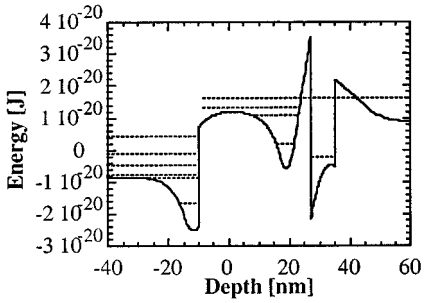

FIG. 4. Band diagram and position of the maxima of the local density of states for the delta-doped HFET structure with additional Si planar top layer on top. The maxima are only given in that part of the structure where the wave function is maximum.

doped electron supply layer and planar doped top layer. The simulations were performed at 77 K. The band diagram and the bound, quasibound, or local states are displayed in Fig. 4. Due to the high barriers in the band diagram of the conventional uniformly doped HFET the states are strongly localized. In the case of the delta-doped HFET with top delta doping the states are no longer localized due to the removal of the top heterojunction barrier and the reduction of the 2DEG/electron supply layer heterojunction barrier.

The access resistance for the structures 1–4 is shown in Table I. The values for the horizontal conductivity are obtained by multiplying the simulated carrier density with the mobility of the respective layers and the electron charge. The vertical resistivity was obtained by quantum-mechanical simulation. The total resistance is a combination of these values. The results clearly show that the total resistance can become considerably smaller than the 2DEG resistance value. From this table, one also notices the bad effect of a high vertical resistance on the total resistance, as for structures 2 and 3. The vertical current density and resistance as a function of bias for structures 1 and 4 are shown in Fig. 5. The vertical resistance of the double delta-doped structure is nearly ten times lower than the resistance of the uniformly doped HFET structure. The standard deviation relative to the mean value for the studied interval ($[-2$ mV, $+2$ mV$]$) is 7% for the new structure and 45% for the conventional HFET structure. Especially toward the drain side (positive voltages), very good linearity is obtained. At the source side the linearity is worse due to the saturation of the heterojunction barrier height separating the 2DEG from the supply layer as a function of bias. At high current densities, as observed in

TABLE I. Calculated resistances at 77 K for the three parallel paths assuming 2500, 1500, and 20 000 $cm^2/V\,s$ as mobility for the top layer, supply layer, and 2DEG, respectively. The total access resistance is a combination of these parallel paths.

	Structure 1 (mΩ/mm)	Structure 2 (mΩ/mm)	Structure 3 (mΩ/mm)	Structure 4 (mΩ/mm)
Top layer	122	115	116	102
Supply layer	752	936	921	590
2DEG	124	116	100	94
Vertical	132	234	535	14
Total	76	80	81	48

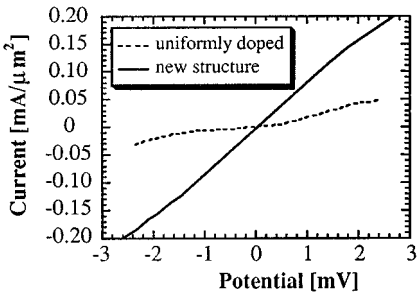

FIG. 5. Current vs potential for a conventional uniformly doped HFET structure and the delta-doped HFET structure with additional Si planar doped top layer.

the double delta-doped structure, the barrier height causes saturation of the source current, whereas for the conventional structure the expected diode behavior is obtained.

IV. MODELING OF THE TEMPERATURE BEHAVIOR

The modeling of the temperature behavior is an interesting way to analyze the rate of tunneling current versus thermionic current through the structure. The tunneling current depends mainly on the density of states and depends barely on temperature. The thermionic current, on the contrary, depends strongly on temperature and is nonexistent at low temperatures when high barriers are to be overcome.

The structure under consideration is a delta-doped HFET with 5 nm $In_{0.25}Ga_{0.75}As$ top quantum well. This structure was chosen because the top heterojunction barrier prohibits carriers from tunneling through this thick barrier and so reduces the total current. At room temperature, however, the transport is expected to be mainly thermionic current over the barrier, so the difference between the room and the liquid-nitrogen current is the thermionic current.

For the analyzed structure, one can see in Fig. 6(a) that the interaction between the 2DEG and the top contact side is very loose, due to the reduced tunneling through the structure. The connection with the back contact is very strong as the local density of states is raised by two decades upon reaching the corresponding energy level (at about 55 meV). The interaction between the 2DEG and the electron supply layer is strong as can be seen in Fig. 6(b). This strong interaction can even contribute to the delocalization of the normally local states. This delocalization or resonance is shown in Fig. 6(b) at an energy of about 106 meV.

When comparing the position of the strongly localized bound and quasibound states with the reference energy chosen in the middle between the left- and right-hand-side conduction-band energies, one observes that this position does not change with temperature. The difference in energy between the conduction bands in equilibrium, however, increases with temperature and so does the position of the local states. This is in agreement with the theory which claims that the temperature does not affect the already filled states, e.g., the bound and quasibound states, but affects the filling of the states around and above the Fermi level. Although it can be argued that when the position of the conduction bands on either side of the heterostructure moves, the bound and quasibound states should follow the changes. It is shown in Fig. 7 that the difference in energy is minimum (about zero) in the layers which contain the bound (-15 to -10 nm) or quasibound states (17 to 23 nm and 27 to 35 nm). The position of these filled states fully determines the equilibrium condition for this structure. The heterojunction FET structure in the access regions is screened off from its contacts and reacts as a closed system to external forces such as current or temperature. These external forces will barely change the equilibrium achieved by the filled states and their interaction.

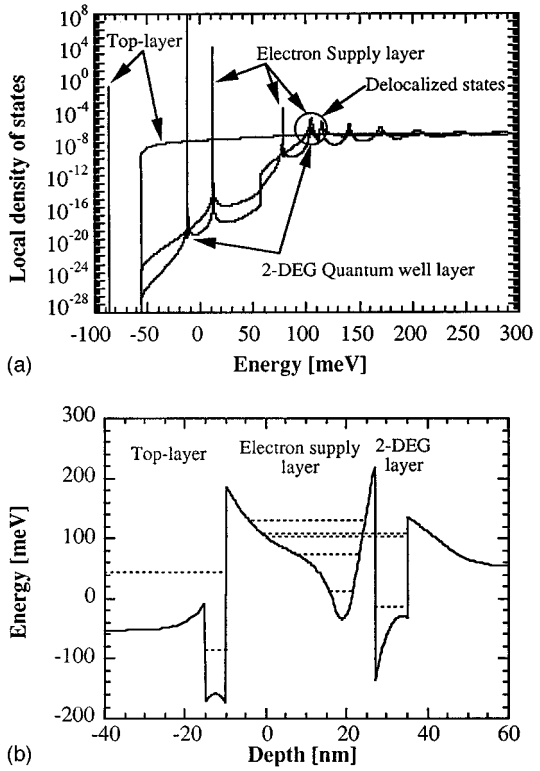

FIG. 6. (a) Local density of states as a function of energy for the top layer, electron supply layer, and 2DEG quantum-well layer for a delta-doped HFET structure with top quantum well. (b) Band diagram and position of the maxima of the local density of states for the delta-doped HFET structure with top quantum-well structure. The position of a maximum is only given in that part of the structure where the wave function reaches its maximum.

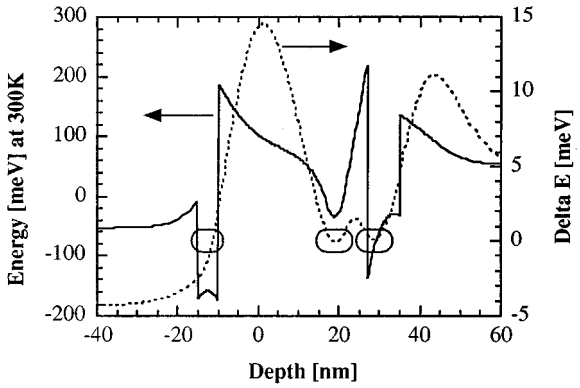

FIG. 7. Band diagram for a delta-doped HFET structure with top quantum-well structure at 300 K and difference in energy with the band diagram for the same HFET structure at 77 K.

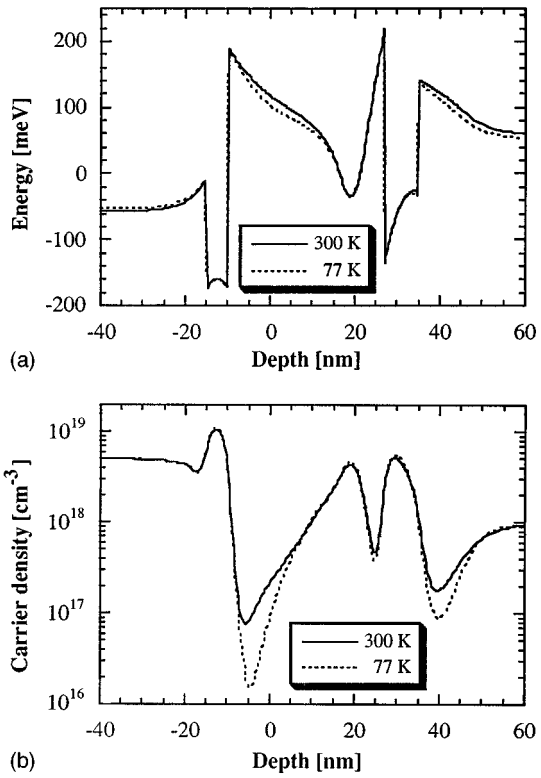

FIG. 8. (a) Band diagram and (b) carrier density for a delta-doped HFET structure with top quantum-well structure at 300 and 77 K.

The differences in band structure and carrier density can be seen in Figs. 8(a) and 8(b), respectively. Although few differences can be seen in the plot of the band diagram, major differences are observed for the carrier densities in and around the heterojunction barriers. By thermionic emission the carrier density in the top heterojunction barrier is enhanced by a factor of 5. The density in the heterojunction barrier between the 2DEG and the GaAs substrate is increased by a factor of 2. At the very thin 2DEG/electron supply layer barrier the density is only increased by about 20%, as most current was already tunneling through it.

V. CONCLUSIONS

In this article the influence of the layer structure on access resistance has been studied using both drift-diffusion and quantum-mechanical models. The addition of a planar doped layer on top of the GaAs/AlGaAs heterojunction improved the carrier density in the top layer significantly without reduction of the vertical tunneling current. The vertical current depended strongly on the AlGaAs/2DEG heterojunction barrier height, which can be reduced by using a Si planar doped AlGaAs electron supply layer. A layer structure with planar doped top heterojunction layer and AlGaAs electron supply layer have been shown to be the best structure for low access resistance.

The current–voltage characteristics and the resistance of two realistic diode structures, a conventional uniform doped HFET and a double delta-doped HFET, have been analyzed using a quantum-mechanical simulation model. The latter structure showed a current density across the structure which is a factor of 10 larger than the conventional structure. Moreover the analysis of the linearity of the resistance as a function of bias is reduced from 45% for the conventional structure to 7% for the double delta-doped structure at 77 K.

The temperature behavior of the heterojunction diodes contributed to the understanding of the physical phenomena occurring in these structures. Increase of the temperature leads to a strong increase of the thermionic/diffusion current over the heterojunction barriers, whereas this current was negligible at liquid-nitrogen temperature. These heterostructures, as they occur in the access region of HFETs, maintain their equilibrium and oppose each change at their contacts. For temperature changes from liquid-nitrogen temperature to room temperature it has been shown that filled bound and quasibound states in the heterostructure determine this equilibrium and that mainly the energy levels of the contact layers have to change to accommodate the difference in structural parameters.

ACKNOWLEDGMENTS

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