A Triple-Well Resonant-Tunneling Diode for Multiple-Valued Logic Application

T. TANOUE, H. MIZUTA, AND S. TAKAHASHI

Abstract—**A new resonant-tunneling diode with four potential barriers and three quantum wells is fabricated and applied to multiple-valued logic for the first time. The diode exhibited significant double negative resistance characteristics and operated as a triply stable device with a single supply voltage between 180 and 230 K.**

I. Introduction

RESONANT tunneling in double-barrier (DB) heterostructures [1] has attracted considerable interest [2], [3]. Several device schemes [4]–[7] utilizing negative differential resistance (NDR) in the DB structures have been proposed as new functional devices. Among these device applications is a multiple-valued logic [6], [7]. For this application, multiple NDR characteristics in which the largest valley current does not exceed the smallest peak current are required (see, for example, [8]); however, it is difficult to obtain this type of current–voltage (I–V) characteristic from DB structures. One of the approaches to avoid this difficulty is to use two DB diodes in parallel with external bias [7]. This approach has the capability of changing I–V characteristics by means of external bias, though the circuit becomes more complex than that for a single diode. In this letter, we present a new approach to realize multiple-valued logic by multiple NDR in a single diode.

II. Device Operation

The difficulty in obtaining the required multiple NDR characteristics from DB diodes is mainly caused by so-called excess current I_{ex}, which increases rapidly as the applied bias increases. As the second NDR, i.e., the second resonance, of DB diodes occurs at much higher voltage than the first one, the second valley current becomes larger than the first peak current, due to I_{ex}. Therefore, in order to realize the required multiple NDR for multiple-valued logic, it is necessary to reduce I_{ex} and/or to lessen the second resonance voltage to the extent that I_{ex} is negligible in comparison to the resonant tunneling current. It is difficult, however, to design a structure in which I_{ex} can be reduced because the origin of I_{ex} has not been made clear at present. Consequently, the second resonance voltage must be reduced.

We propose a new resonant tunneling structure in which two resonance voltages can be controlled separately, thus leading to the realization of multiple-valued logic function in a single diode. The structure consists of three quantum wells, named $W1$–$W3$, and four potential barriers as shown in Fig. 1(a). Also shown in the figure are calculated quasi-eigen energies, named E_1–E_3, and existent probabilities of electrons at these energies. It should be noted that the thickness of the three wells L_{W1}–L_{W3} are chosen to have a relation $L_{W1} > L_{W3} > L_{W2}$, so that the electrons at E_1 are mainly located in $W1$, those at E_2 in $W3$, and those at E_3 in $W2$. Although this structure is a coupled three-well quantum mechanical system, it is found by our calculation that the energy E_1 is, analogous to the case of a single quantum well, mainly determined by L_{W1} because of the location of electrons as mentioned above; similarly, the energies E_2 and E_3 are determined by L_{W3} and L_{W2}, respectively. When an external bias is applied, the voltage drop is expected to take place not in $W1$ but mostly in $W2$ and $W3$ because electrons injected from the cathode layer cancel electric field in $W1$; furthermore, the energies E_2 and E_3 are expected to change with the energy of the bottom of $W3$

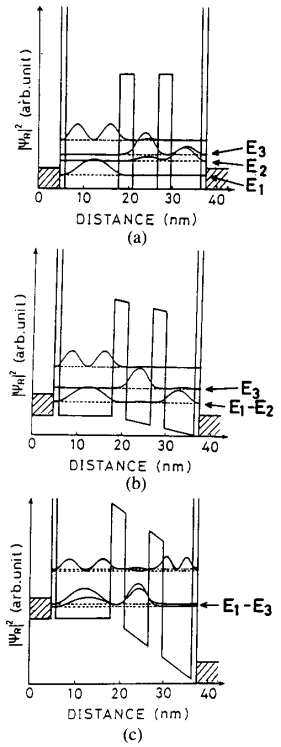


Fig. 1. Conduction-band diagrams of a triple-well resonant tunneling structure with (a) zero bias, (b) first resonance condition, and (c) second resonance condition. Quantized levels are shown by horizontal lines. Existent probabilities of electrons are also shown. It can be clearly seen from existent probability that resonances are taking place in (b) and (c).

Manuscript received February 19, 1988; revised May 25, 1988.

The authors are with the Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185, Japan.

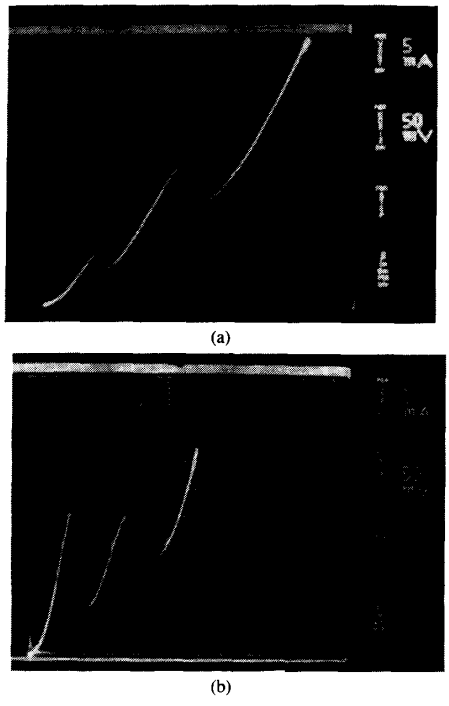
IEEE Log Number 8822493.

and $W2$ because the electrons at E_2 are mainly located in $W3$, and those at E_3 in $W2$. Thus, two kinds of resonance are expected to take place in the structure as shown in Fig. 1: resonances between E_1 and E_2 (Fig. 1(b)) and between E_1 and E_3 (Fig. 1(c)). It is evident that the zero-bias energy difference between E_1 and E_2 mainly determines the first resonance voltage and that between E_1 and E_3 the second resonance voltage. Therefore, since the energies E_2 and E_3 are determined by L_{W3} and L_{W2}, the two resonance voltages can be adjusted independently by L_{W2} and L_{W3}. It is actually shown by our calculation that the resonance voltages can be controlled independently by L_{W2} and L_{W3}. The detail of the calculation, however, is not in the scope of this letter and will be described elsewhere [10]. This independent adjustability of the two resonance voltages is the advantage of this structure compared to DB or triple-barrier (TB) structures [11], in which the two voltages are determined simultaneously by the energies of the ground and the excited levels in a single quantum well. In contrast to the DB or TB structures, the existence of three wells in this structure is necessary and sufficient for controlling the two resonance voltages; therefore, we call this structure a triple-well resonant tunneling structure. Although quantum-well structures with more than two barriers have been analyzed [12]. [13], this is the first time, to the authors' knowledge, that the structure is applied to multiple-valued logic.

III. Experimental

The samples used for experimental demonstration were grown using a conventional molecular beam epitaxy system with elemental Ga, Al, As, and Si as source materials. On a Si-doped (100) GaAs substrate, the following layers were successively grown: a 500-nm Si-doped ($1 \times 10^{18}/cm^3$) GaAs buffer layer, a 10-nm GaAs spacer layer, a triple-well structure consisting of 1 nm of AlAs, 6.9 nm of GaAs, 3 nm of $Al_{0.26}Ga_{0.74}As$, 5.7 nm of GaAs, 3 nm of $Al_{0.26}Ga_{0.74}As$, 11.9 nm of GaAs, and 1 nm of AlAs, and, finally, a 300-nm Si-doped ($1 \times 10^{18}/cm^3$) GaAs layer. The layer thicknesses and the doping concentration were determined by numerical simulation whose details will be described elsewhere [10]. All the layers are unintentionally doped (typically p-type with a hole concentration of $1 \times 10^{14}/cm^3$ for GaAs) unless otherwise noted. Growth was interrupted for 3 min at each interface between different materials. The wafer was processed by conventional photolithography and wet chemical etching to define diode areas, followed by a deposition of AuGe alloy, lifting off, and sintering at 400°C for 2 min in N_2 gas ambient to form ohmic contacts. As a reference, DB diodes with two 1.5-nm-thick AlAs barriers and a 4.5-nm-thick GaAs well were grown and processed in the same manner. The I–V characteristics of the diodes were measured by a Tektronix 576 curve tracer connected with a variable temperature automatic prober. The sample temperature was varied between room temperature and 85 K.

From a reference DB diode, resonant-tunneling current density of $1.2 \times 10^5 A/cm^2$ was observed with a peak-to-valley current ratio between 1.6 and 2.4 in the entire temperature range. The current density is, to our knowledge, the highest ever reported for this material system, indicating the good quality of our MBE material and the appropriateness of the fabrication process. Significant double NDR was observed from the triple-well diodes even at room temperature, as shown in Fig. 2(a). Cooling the sample down to 219 K resulted in the reduction of the second valley current, as shown in Fig. 2(b), realizing a I–V curve applicable to a triple-valued logic. Even though double NDR was observed from some of the DB or TB diodes fabricated at the same time, with the second valley current always being more than an order of magnitude larger than the first peak in the whole temperature range, they could not be applied to a triple-valued logic. With a load resistance of 100 Ω and applied voltage of 1 V, it is expected from Fig. 2(b) that this diode should exhibit stable states at 0.065, 0.155, and 0.250 V. The experimentally observed values were 0.066, 0.158, and 0.249 V, which showed excellent agreement with the expected ones. Since the second current peak diminished with further decreases of temperature, double NDR and tri-stable operation were not observed for the sample temperature below 180 K.



(a)

(b)

Fig. 2. Current–voltage characteristics of triple-well diodes exhibiting significant multiple negative resistance (a) at room temperature and (b) at 219 K.

IV. Discussion

Numerical simulation of I–V characteristics of triple-well diodes was performed using potential profiles as shown in Fig. 1, and the results were compared with the experiment. In spite of a rather rough approximation for the potential profile, numerically simulated peak voltages showed good agreement with the experimentally observed values, though the former is slightly lower than the latter in most cases. This slight difference can be attributed to series resistances of the diodes and the external circuit because the discrepancy between the

simulation and the experiment decreases for diodes with smaller area, i.e., for smaller diode currents that should lead to smaller voltage drops at the external circuit.

In contrast to the good agreement between the predicted and the observed peak voltages, the peak current density of the triple-well diode, which was 500 A/cm^2 at most, was more than an order of magnitude lower than what was given by our numerical simulation; furthermore, the temperature dependence of the current density was also much stronger than the prediction. In DB diodes, contrastingly, the disagreement between the experimental results and the simulated values was not more than a factor of 3, which indicates that the tunneling current in triple-well diodes is limited by some factors that can be neglected in DB diodes. Though what limits the tunneling current is not completely clear at present, it was found that the discrepancy tends to become larger for thicker resonant tunneling structures. From this observation, it is suspected that random scattering of electrons takes place during the tunneling process, thus reducing the tunneling probability of electrons and changing the temperature dependence of the tunneling current. Work is now underway to develop a new simulation of NDR characteristics in resonant tunneling structures which takes random scattering of electrons into consideration.

Acknowledgment

The authors thank M. Kobayashi and Dr. H. Yanazawa and his staff for device fabrication, C. Kusano for his help in low-temperature measurement, and Dr. H. Matsumura for encouragement.

References

[1] L. L. Chang, L. Esaki, and R. Tsu, "Resonant tunneling in semiconductor double barrier," *Appl. Phys. Lett.*, vol. 24, pp. 593–595, 1974.

[2] T. C. Sollner, W. D. Goodhue, P. E. Tannenwald, C. D. Parker, and D. D. Peck, "Resonant tunneling through quantum wells at frequencies up to 2.5 THz," *Appl. Phys. Lett.*, vol. 43, pp. 588–590, 1983.

[3] T. J. Schewchuk, P. C. Chapin, P. D. Coleman, W. Kopp, R. Fischer, and H. Morkoç, "Resonant tunneling oscillation in a GaAs-$Al_xGa_{1-x}As$ heterostructure at room temperature," *Appl. Phys. Lett.*, vol. 46, pp. 508–510, 1985.

[4] N. Yokoyama, K. Imamura, S. Muto, S. Hiyamizu, and H. Nishi, "A new functional resonant tunneling hot electron transistor (RHET)," *Japan J. Appl. Phys.*, part 2, vol. 24, pp. L583–L584, 1985.

[5] A. R. Bonnefoi, T. C. McGill, and R. D. Burnham, "Resonant tunneling transistors with controllable negative differential resistance," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 636–638, 1985.

[6] F. Capasso, S. Sen, A. C. Gossard, A. L. Hutchinson, and J. H. English, "Quantum well resonant tunneling bipolar transistors operating at room temperature," *IEEE Electron Device Lett.*, vol. EDL-7, pp. 573–576, 1986.

[7] F. Capasso, S. Sen, A. Y. Cho, and D. Sivico, "Resonant tunneling devices with multiple negative differential resistance and demonstration of a three-state memory cell for multiple-valued logic applications," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 297–299, 1987.

[8] C. Rine, Ed., *Computer Science and Multiple-Valued Logic.* Amsterdam: North-Holland, 1984, p. 415.

[9] A. Harwit, J. S. Harris, Jr., and A. Kapitulnik, "Calculated quasi-eigenstates and quasi-eigen energies of quantum well superlattices in an applied electric field," *J. Appl. Phys.* vol. 60, pp. 3211–3213, 1986.

[10] H. Mizuta, "A new triple well resonant tunneling diode with controllable double negative resistance," to be published.

[11] T. Nakagawa, H. Imamoto, T. Kojima, and K. Ohta, "Observation of resonant tunneling in AlGaAs/GaAs triple barrier diodes," *Appl. Phys. Lett.*, vol. 69, pp. 73–75, 1986.

[12] R. Tsu and L. Esaki, "Tunneling in a finite superlattice," *Appl. Phys. Lett.*, vol. 22, pp. 562–564, 1973.

[13] C. J. Summers and K. R. Brennan, "Variably spaced superlattice energy filter, a new device design concept for high-energy electron injection," *Appl. Phys. Lett.*, vol. 48, pp. 806–808, 1986.