Energy-balance modelling of short channel single-GB thin-film transistors

Philip M. Walker*

Microelectronics Research Centre,
University of Cambridge,
Cambridge CB3 0HE, UK
E-mail: pmw35@cam.ac.uk
*Corresponding author

Hiroshi Mizuta

School of Electronics and Computer Science,
University of Southampton, Southampton SO17 1BJ, UK
Department of Physical Electronics,
Tokyo Institute of Electronics, Tokyo 152-8552, Japan
E-mail: mizuta@pe.titech.ac.jp

Abstract: In this paper, we have investigated the effect of a single Grain Boundary (GB) on the performance of decananometer-scale Thin Film Transistors (TFTs) by using the calibrated energy balance transport model and a continuous trap state distribution at the GB. We have found that the GB potential barrier suppresses the subthreshold slope and leakage current in devices, where the DIBL effect and punchthrough currents significantly degrade device performance. We have also found that the drift-diffusion model underestimates the drain current in the single-GB TFT and the velocity overshoot effect becomes significant in the short channel regime. Inclusion of trap-to-band and band-to-band tunnelling models into our simulations have shown that the subthreshold leakage current has a significant field dependence in the negative gate bias regime.

Keywords: poly-silicon; grain boundary; energy-balance modelling; thin-film transistor.

Reference to this paper should be made as follows: Walker, P. M. and Mizuta, H. (2006) 'Energy-balance modelling of short channel single-GB thin-film transistors', *Int. J. Computational Science and Engineering*, Vol. 2, Nos. 3/4, pp.148–157.

Biographical notes: P.M. Walker is a Research Student at the University of Cambridge. His PhD research has been to study the potential applications of polycrystalline silicon for use in advanced submicron thin-film transistors. He received his BEng (Hons) from the University of Glasgow in 2001 and his final year dissertation concerned the fabrication and simulation of InP resonant tunnelling diodes.

Hiroshi Mizuta is a Professor of Nanoelectronics at the School of Electronics and Computer Science at the University of Southampton and a Professor at Department of Physical Electronics, Tokyo Institute of Technology. His current research interests are Si nanodots and nanowires, electron transport in Si nanostructures, ab-initio calculations of nanomaterial properties and quantum transport and their novel applications to quantum information devices and nano electromechanical devices. He has co-authored more than 200 scientific papers and filed over 50 patents. He has also co-authored books and chapters, including *Physics and Applications of Resonant Tunnelling Diodes*, Cambridge University Press, 1995.

1 Introduction

Polysilicon Thin-Film Transistors (TFTs) have been studied extensively in recent years for their use in flat panel active matrix displays. When polysilicon TFTs are used in AMLCD applications, the minimum feature size is typically very large (in the order of tens of microns), and therefore a large number of Grain Boundaries (GBs) are present in the channel. When modelling such devices, conventionally, reducing the average carrier mobility below the bulk-single crystal value includes the effect of the GBs. In such an analysis the discrete properties of individual GBs are not considered. More recently the polysilicon has been proposed as a device material for use in 3D VLSI circuits (Banerjee et al., 2001). For the future 3D integration of VLSI devices the channel length must be scaled to much smaller dimensions. In scaling the channel of the device down to the decananometre regime – a length and width comparable to the polysilicon grain size – it is important to understand the effects of discrete GBs on conduction (Yamaguchi, 2001).

When the poly-Si film is fabricated using Solid Phase Crystallisation (SPC) of deposited a-Si, the grain size is usually only in the order of hundreds of nanometres or less (Subramanian et al., 1997). Therefore, when using SPC films to fabricate TFTs, it follows that if we scale the transistor down to the short channel regime – that is channel length less than one micron – only a small number of GBs will be present in the device channel (Jeon et al., 2001; Oh and Matsumura, 2001). Therefore it is increasingly important to understand the effects of discrete GBs on carrier transport.

In our previous work (Walker et al., 2004) we modelled a TFT with a single grain boundary located at the centre of the channel and oriented perpendicular to the direction of current flow. We showed that improvements in the subthreshold slope and leakage current were possible in short channel single-GB TFTs, relative to their SOI equivalents.

To perform the simulation we used a 2D drift diffusion model, with a localised trap model where the traps were located only at the GB region. Generation and recombination processes from the traps were simulated using Shockley-Read-Hall statistics and the traps were assumed to be mono-energetic and located close to the middle of the forbidden energy gap.

In this work we seek to improve the realism of the simulation model used in Walker et al. (2004) and to thereby validate it's conclusions. There are two key improvements that can be made to the simulation model.

Firstly, instead of using mono-energetic traps, we include distribution of traps across the energy band gap, where the distribution is based on experimental measurements.

Secondly, we can use the Energy-Balance (EB) model instead of the conventional Drift-Diffusion (DD) model. This is especially important as the channel lengths are scaled into the decananometer regime because of hot carrier effects.

Finally, we can include additional generation and recombination effects due to the tunnelling of carriers directly from the valence band to the conduction band or via the trap states in high electric fields. This is important as in the high electric fields found in a short channel device additional current due to tunnelling can be significant.

Currently, we do not model quantum mechanical effects such as phonon limited electron mobility, reduction in inversion layer charge or direct tunnelling from the source to the drain.

2 Simulation model

2.1 EB model

Previously, we used the basic DD formulation of the semiconductor device equations. These assume that the carrier temperatures are in equilibrium with the surrounding crystal lattice. Thus, not taking into account the possibility of non-equilibrium transport, that can occur when strong electric fields are present in short channel devices. The high electric fields can cause substantial heating of carriers, resulting in carrier energies, which far exceed those of equilibrium. The velocity overshoot effect occurs when carriers in large electric fields are accelerated to velocities larger than the equilibrium saturation limit. Not including this effect can lead to underestimation of the drain currents in MOSFET simulations. It has been estimated that these effects can become significant in MOSFETs with channel lengths less than ≈100 nm (Snowden, 1988). Therefore, for accurate simulation of devices in this regime, an extended DD model derived from the higher order moments of the Boltzmann equation is often used; this incorporates, carrier temperature/energy, as a further transport parameter. One model using this approach is the energy balance model (Stratton, 1962, 1972) and it is incorporated into the (ATLAS User's Manual, 2002) device simulation package, which we use for all the simulations presented in this paper.

The energy balance model consists of a set of six coupled partial differential equations, which are for energy balance, current density $\overrightarrow{J_{n,p}}$ and energy flux $\overrightarrow{S_{n,p}}$ for both holes and electrons, respectively.

Assuming Boltzmann statistics, then for electrons these consist of:

$$\nabla\overrightarrow{S_n} = \frac{1}{q}\overrightarrow{J_n}\overrightarrow{E} - \frac{3kn}{2}\frac{T_n - T_L}{\tau_e^n} - W_n \tag{1}$$

$$\overrightarrow{J_n} = qD_n\nabla n - q\mu_n n\nabla\phi + qnD_n^T\nabla T_n \tag{2}$$

$$\overrightarrow{S_n} = -K_n\nabla T_n - \left(\frac{3}{2}\frac{k}{q}\right)\overrightarrow{J_n}\,T_n \tag{3}$$

and for holes:

$$\nabla\overrightarrow{S_p} = \frac{1}{q}\overrightarrow{J_p}\overrightarrow{E} - \frac{3kp}{2}\frac{T_p - T_L}{\tau_e^p} - W_p \tag{4}$$

$$\overrightarrow{J_p} = qD_p\nabla p - q\mu_p p\nabla\phi + qnD_p^T\nabla T_p \tag{5}$$

$$\overrightarrow{S_p} = -K_p\nabla T_p - \left(\frac{3}{2}\frac{k}{q}\right)\overrightarrow{J_p}\,T_p \tag{6}$$

where two independent variables T_n and T_p have been used for the electron and hole temperatures, respectively, T_L is the lattice temperature and $\tau_e^{n,p}$ are the energy relaxation times for electrons and holes, respectively. The energy flux densities for electrons and holes are given as $\overrightarrow{S_n}$ and $\overrightarrow{S_p}$. D_n and D_p are the temperature dependent diffusivities given by

$$D_n = \frac{\mu_n kT_n}{q} \tag{7}$$

$$D_p = \frac{\mu_p kT_p}{q} \tag{8}$$

K_n and K_p are the thermal conductivities where all for electrons and holes, respectively given by

$$K_n = qn\mu_n\left(\frac{3}{2}\frac{k^2}{q^2}\right)T_n \tag{9}$$

$$K_p = qp\mu_p\left(\frac{3}{2}\frac{k^2}{q^2}\right)T_p \tag{10}$$

W_n and W_p are the energy density loss rates. If we consider only Shockley-Read-Hall recombination processes then the energy density loss rates can be expressed as:

$$W_n = \frac{3}{2}n\frac{k\left(T_n - T_L\right)}{\tau_e^n} + \frac{3}{2}kT_nR_{\text{srh}} \tag{11}$$

$$W_p = \frac{3}{2}p\frac{k\left(T_p - T_L\right)}{\tau_p^n} + \frac{3}{2}kT_pR_{\text{srh}} \tag{12}$$

The energy relaxation time governs the magnitude of the non-stationary transport effects such as velocity overshoot, therefore it is a critical parameter in the energy balance model. In the next section, we show a method of finding accurate estimates of $\tau_e^{n,p}$ using Monte-Carlo simulations.

2.2 *Calibration of energy relaxation times using Monte-Carlo simulation*

The energy relaxation time $\tau_e^{n,p}$ for electrons and holes is a critical parameter in the energy balance scheme of equations. It is a measure of the amount of time needed for the carrier energy to reach equilibrium with the electric field. The larger the relaxation time the greater the magnitude of the non-stationary effects. In the classical DD model, this time is assumed to be zero and the maximum carrier velocity is given by the velocity saturation limit. In the energy balance regime the velocity can overshoot this value before returning to the equilibrium level after a finite time; this is the energy relaxation time.

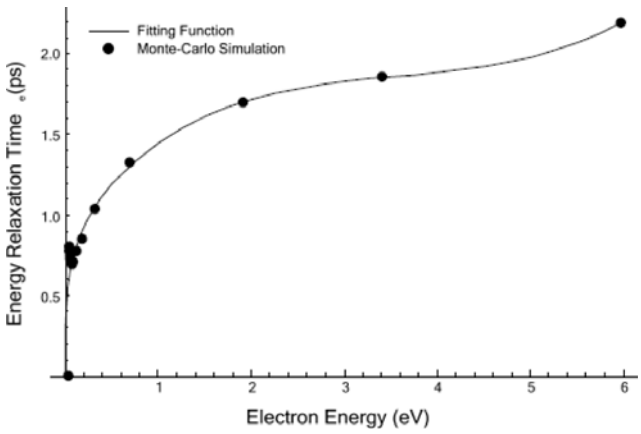
The default model in ATLAS assumes a constant relaxation time for both holes and electrons of 0.25 ps. The value of the relaxation time is controversial, as it is not directly measurable and incorrect values can lead to non-physical behaviour in the simulations. Furthermore, the relaxation time is not constant but varies with carrier energy. The best approach, to determine suitable values for the carrier relaxation times, is to use bulk Monte-Carlo simulations to evaluate the ensemble average value. We use the commercial Monte-Carlo simulator 'MOCASIM' (MOCASIM User's Manual, 2002). In this simulation, a finite number of electrons are generated in equilibrium at a specific field, doping and temperature. The system is allowed to evolve from an initial distribution and how it changes with time is evaluated by calculating the scattering of the carriers at each time step. The allowed scattering mechanisms are specified in the simulation input file and the process continues until the carrier distribution converges to a steady state. It is at this point that the transport parameters can be extracted, by taking the average of the ensemble.

The parameters used in our simulation are summarised in Table 1. In the Monte-Carlo simulations the silicon is assumed to be intrinsic, therefore no doping dependency is currently incorporated into the model. The extracted relaxation time for electrons against carrier energy is plotted in Figure 1, along with a curve fitted using an arbitrary function. The carrier energy dependence of the energy relaxation time is then incorporated into the device simulations by modifying the energy balance model to use the function of the curve fit to evaluate the relaxation time for each mesh node. It was found that using our energy dependent relaxation time also helped ATLAS converge to a solution when using the EB model.

Table 1 Table of parameters for the Monte-Carlo simulation of intrinsic silicon

Simulation parameter	*Parameter value*		
Number of carriers	1000		
Doping density	1×10^{11} cm^{-3}		
Number of time steps	20, 000		
Time step	1×10^{-15} s		
Scattering mechanism	*Intervalley phonon energy*	*Deformation potential*	*Number of valleys*
Acoustic phonon scattering	N/A	9.5 V/cm	N/A
Intervalley phonon scattering (X->X)	0.01206 eV	0.50×10^8 V/cm	2
	0.01810 eV	0.80×10^8 V/cm	2
	0.06032 eV	3.00×10^8 V/cm	2
	0.01810 eV	0.15×10^8 V/cm	2
	0.04309 eV	2.50×10^8 V/cm	2
	0.05429 eV	4.00×10^8 V/cm	2
Ionised impurity scattering	N/A	N/A	N/A

Figure 1 Energy relaxation time $\grave{A}\tau_e$ plotted against electron energy for intrinsic silicon. An arbitrary function was fitted to the data points supplied by the Monte Carlo simulation to approximate the temperature dependence of the relaxation times in the energy balance model



2.3 *Modelling of grain boundary trap states*

To model the inclusion of trap states in the forbidden gap the space charge term on the right-hand side of Poisson's equation is modified by including an additional charge term Q_T representing trapped charge. This is given by

$$-\rho = q\left(p - n + N_D^+ - N_A^-\right) + Q_T \tag{13}$$

$$Q_T = q\left(p_T - n_T\right) \tag{14}$$

where N_D^+ and N_A^- are the ionised donor and acceptor concentrations, respectively and p_T and n_T are the trapped hole and electron concentrations, respectively. We assume that the trap states consist of both donor- and acceptor like states distributed across the forbidden energy gap, where the donor-like states act as hole traps and the acceptor-like traps act as electron traps. Therefore the total density of states is given by

$$g(E) = g_D(E) + g_A(E) \tag{15}$$

where $g_D(E)$ is the total density of donor-like trap states and $g_A(E)$ is the total density of acceptor-trap states. To calculate the trapped charge we perform a numerical integration of the product of the trap density and its occupation probability over the forbidden energy gap. This gives

$$n_T = \int_{E_V}^{E_C} g_A(E) f_A(E,n,p) dE \tag{16}$$

$$p_T = \int_{E_V}^{E_C} g_D(E) f_D(E,n,p) dE \tag{17}$$

for trapped electrons and holes, respectively, where f_A and f_D are the occupation probability for acceptor-like and donor-like traps.

The occupation probabilities are then given by

$$f_A = \frac{v_n \sigma_{\text{ae}} n + v_p \sigma_{\text{ah}} p_t}{v_n \sigma_{\text{ae}} (n + n_t) + v_p \sigma_{\text{ah}} (p + p_t)} \tag{18}$$

$$f_D = \frac{v_n \sigma_{de} n + v_p \sigma_{dh} p_t}{v_n \sigma_{de} \left(n + n_t\right) + v_p \sigma_{dh} \left(p + p_t\right)} \tag{19}$$

where σ_{ae}, σ_{ah} and σ_{de}, σ_{dh} are the electron and hole capture cross sections for acceptor-like and donor-like traps, respectively. The effective electron and hole concentrations n_t and p_t are defined as

$$p_t = n_i \exp\left[\frac{E_i - E}{kT}\right] \tag{20}$$

$$n_t = n_i \exp\left[\frac{E - E_i}{kT}\right] \tag{21}$$

where n_i is the intrinsic carrier concentration, E is the trap energy level, E_i is the intrinsic fermi level and T is the lattice temperature.

The Shockley–Read–Hall recombination/generation rate (Hall, 1952; Shockley and Read, 1952) per unit time is modified to include the multiple trap levels and is given by

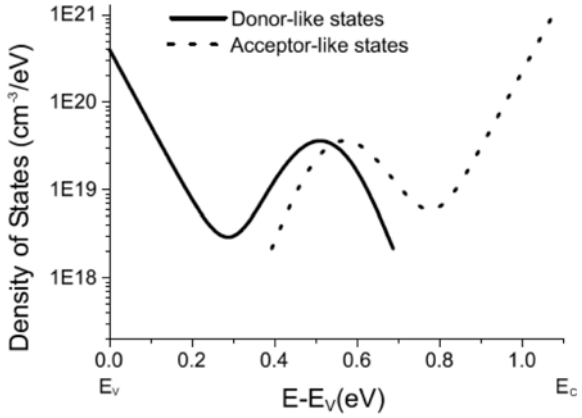
$$U_{n,p} = \int_{E_V}^{E_C} \left(\frac{v_n v_p \sigma_{ae} \sigma_{ah} (np - n_i^2) g_A(E)}{v_n \sigma_{ae} (n + n_t) + v_p \sigma_{ah} (p + p_t)} + \frac{v_n v_p \sigma_{de} \sigma_{dh} (np - n_i^2) g_D(E)}{v_n \sigma_{de} (n + n_t) + v_p \sigma_{dh} (p + p_t)} \right) \tag{22}$$

2.4 Trap state distribution model

As discussed in the introduction, in our previous simulation study (Walker et al., 2004), we assumed that the trap states were mono-energetic. That is, they existed at a fixed point in the energy band gap. Experiment studies have shown that this model is unrealistic and that the traps are in fact spread over the band gap with acceptor-like traps closer to the conduction band and donor-like traps closer to the valence band. The device simulation package ATLAS allows us to define a density of defect states as a combination of four bands. Two tail bands are specified that contain large numbers of defect states at the conduction band (acceptor-like traps) and valence band (donor-like traps) edges, respectively. These both decay rapidly as we move towards the centre of the forbidden energy gap. In addition two deep level bands are defined (acceptor and donor-like) which are modelled using a gaussian distribution with its peak close to the middle of the forbidden energy gap.

However, many different trap density distributions have been proposed to describe the position and density of the traps within the polysilicon band gap. These have consisted of single energy level models (Walker et al., 2004; Yang et al., 1999), models with single (Chern et al., 1995) or double (Armstrong et al., 1997, 1998; Chou and Kanicki, 1999) exponential tail states, gaussian shaped distributions (Kamins, 1998; Kimura et al., 2001a,b) or both (Faughnan and Ipri, 1989; Ikeda, 2002). It has been suggested that the tail states dominate the above threshold behaviour while the mid-gap states primarily effect the subthreshold behaviour (Armstrong et al., 1997; Chern et al., 1995). In this study we are concerned with the both the subthreshold region and the above threshold region. So to ensure a realistic model we chose to include both mid-gap and tail states. The trap density distributions used in our simulation study are plotted in Figure 2 as a function of energy.

Figure 2 The distribution of the acceptor and donor-like trap states across the forbidden energy gap that are used in our simulation study



As it is widely accepted that the trap density distribution contains exponential band tails at the valence and conduction band edges, when deciding on a suitable distribution the main qualitative choice is whether to include the mid-gap states as additional exponential terms

such as in Armstrong et al. (1997, 1998) and Chou and Kanicki (1999) or as gaussian terms as used in Dimitriadis et al. (1993) Dimitriadis and Tassis (1995) and Ikeda (2002). We choose to use gaussian terms; the reason being that the papers dealing with SPC films suggest a peak in trap states near the mid-gap and it is SPC films that we are considering in this work. The values chosen are in the range suggested in Dimitriadis et al. (1993) and are given in Table 2.

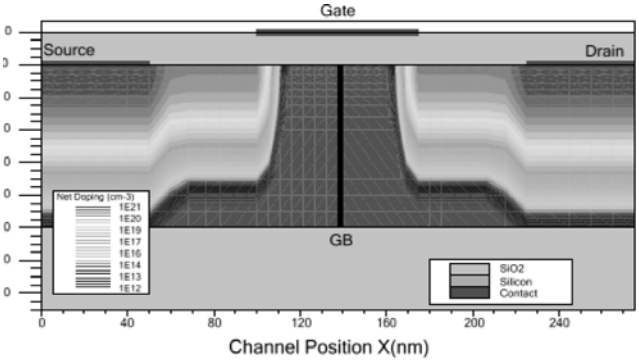
Table 2 Trap state distribution parameters and device structure parameters used in the simulation model

Device Parameter	*Symbol(units)*	*Value*
Channel length	L (nm)	400
Channel width	L (nm)	1000
Gate oxide thickness	t_{ox} (nm)	10
Polysilicon thickness	t_{si} (nm)	25/50
Buried oxide thickness	t_{box} (nm)	25
Source and drain dopant density	n^+ (cm^{-3})	1×10^{21}
Width of grain boundary	W_{gb} (nm)	4
Capture cross section of electrons in acceptor-like states	σ_{ae} (cm^2)	1×10^{-16}
Capture cross section of holes in acceptor-like states	σ_{ah} (cm^2)	1×10^{-14}
Capture cross section of electrons in donor-like states	σ_{de} (cm^2)	1×10^{-14}
Capture cross section of holes in donor-like states	σ_{ae}((cm^2)	1×10^{-16}
Density of acceptor-tail states	N_{TA} (cm^{-3}eV^{-1})	1×10^{21}
Density of donor-tail states	N_{TD} (cm^{-3}eV^{-1})	4×10^{20}
Density of acceptor-gaussian states	N_{GA} (cm^{-3}eV^{-1})	5×10^{19}
Density of donor-gaussian states	N_{GD} (cm^{-3}eV^{-1})	5×10^{19}
Decay energy for acceptor-tail states	W_{TA} (eV)	0.05
Decay energy for donor-tail states	W_{TD} (eV)	0.05
Decay energy for acceptor-gaussian	W_{GA} (eV)	0.1
Decay energy for donor-gaussian	W_{GD} (eV)	0.1
Energy of gaussian for acceptor-states	E_{GA} (eV)	0.51
Energy of gaussian for donor-states	E_{GD} (eV)	0.51

2.5 Device structure

Figure 3 shows the basic device structure we used for the device modelling. In this simple structure we assumed a thin polysilicon layer of t_{si} = 50 nm, this is to facilitate easy comparison with the results for subthreshold behaviour, presented in Walker et al. (2004). A gate oxide of 10 nm is chosen, which we estimate is near limit of the thickness that is possible in polysilicon, due to surface roughness at the oxide-polysilicon interface (Moazzami and Hu, 1993). The source and drain regions are heavily doped n-type material, with a doping density of 1×10^{21}cm^{-3}, while the channel region is intrinsic. In our model there are no trap states located in the grain regions, only in the grain boundary region. In previous simulation studies the GB width has been assumed to be within 1–5 nm, in our simulation it is 4 nm in width which is within this range (Kithahara et al., 2003; Yamaguchi, 2001).

Figure 3 The device structure used in the energy balance simulations, t_{si} = 50 nm, t_{ox} = 10 nm and L = 100 nm. The contour shading denotes the net doping and shows the Lightly Doped Drain (LDD) structure utilised in the device. The doping distribution was modelled using a gaussian distribution



We choose to limit the maximum channel length used in this study to L = 100 nm. This is because 100 nm is close to the limit where the DD model is thought to become inaccurate and is of a magnitude in the order of the size of grains that are typically obtained by SPC of deposited a-Si.

The grains of the polysilicon were assumed to be columnar. In the channel of the modelled device only a single GB was included and oriented so it was perpendicular to the semiconductor interface. The lightly doped source and drain are designed to reduce the electric field at their boundary with the channel and therefore facilitate better immunity to short channel effects such as DIBL. The same structure is used when simulating SOI devices for comparison, with the obvious exception of the traps at the GB region.

3 Simulation results

3.1 Comparison of DD and EB model

The devices simulated had channel lengths of 100 nm and the device structure is as shown in Figure 3. The bias conditions of the simulation were set at V_d = 0.01 and 1.2 V, respectively, the latter value is chosen as this is the power supply voltage specified for low standby power transistor operation in the ITRS (2003).

A comparison of the $I_d - V_g$ characteristics when using the DD model and the calibrated EB model is shown in Figure 4. We observe that the drain currents predicted using the EB model are higher than those when using the DD model. This can be explained by considering the velocity overshoot effect. As previously discussed velocity overshoot is the consequence of the finite time needed for the energy of the carriers to return to their equilibrium values. The velocity overshoot effect is especially

important at high drain bias, as the electric field strength is higher, and therefore non-equilibrium transport effects are significant. In our results, when V_d = 0.01 V the difference in drain currents is smaller in comparison to the difference when V_d = 1.2 V. If we then compare the plots of electron velocity against channel position at 1nm from the semiconductor/oxide interface (Figure 5), we can clearly see that the carrier velocity is much higher, when using the EB model.

Figure 4 An overlay of the $I_d V_g$ characteristics at V_d = 0.01V and 1.2 V for a 100 nm single-GB TFT. A comparison is made between the results from the DD model and the calibrated EB model

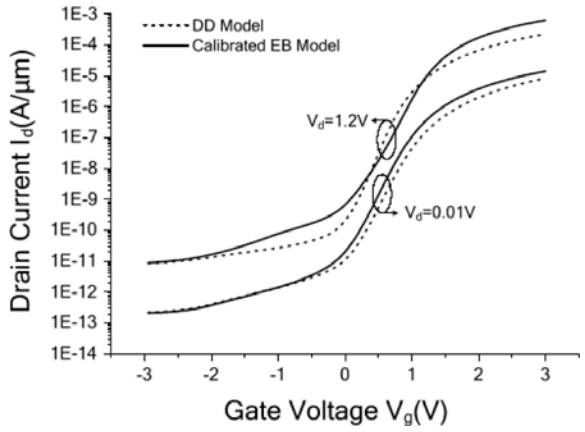
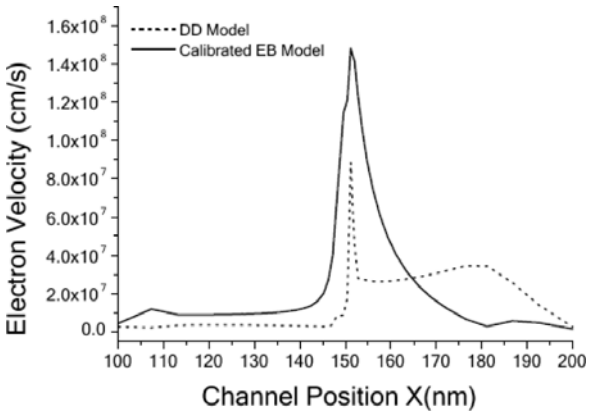


Figure 5 A comparison of the electron velocity in the channel of the single-GB TFT (V_d = 1.2 V and V_g = 3 V) when using the DD or calibrated EB model. The max electron velocity is higher when using the EB model due to the velocity overshoot effect



This is as a direct consequence of the velocity overshoot effect and this is the reason for the increased drain current. The I_d–V_d characteristics are shown in Figure 6. These provide further clear illustration of the larger drain currents that result when using the EB model.

3.2 Validation of improved subthreshold behaviour

We then investigated if the trend towards improved subthreshold behaviour compared to the SOI equivalent is still found when using the EB model. Both single-GB TFT and equivalent SOI devices were simulated, using the same structure as before and with channel lengths of 100 nm, 75 nm, 65 nm and 53 nm. Convergence time for simulating single-GB TFTs was found about 3–4 times as long as that for SOI devices as a result of including the modelling of the GB traps. Default convergence criteria parameters set in ATLAS were adopted, that are enough for most purposes. The I_d–V_g characteristics of the simulated devices are shown in Figures 7 and 8, for V_d = 0.01 V and 1.2 V, respectively.

Figure 6 An overlay of the I_d–V_d characteristics at V_g = 1 V, 2 V, 3 V, 4 V for a 100nm single-GB TFT. Comparison between the results from the DD model and the calibrated EB model show that larger drain currents result when the EB model is used

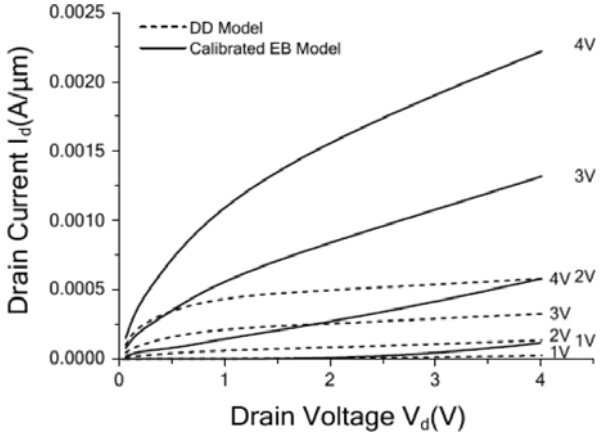
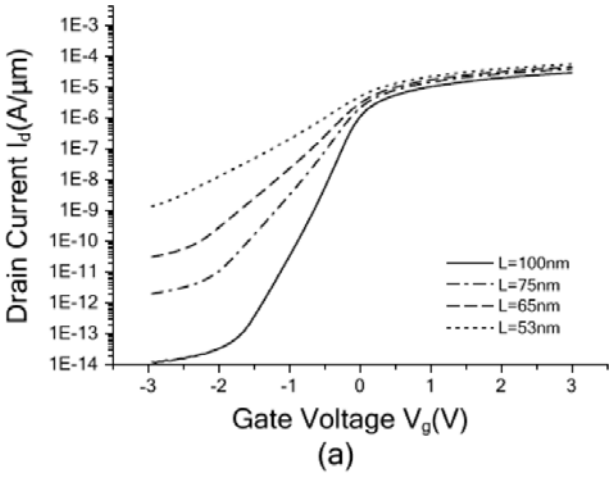


Figure 7 I_d–V_g characteristics at V_d = 0.01 V for (a) SOI and (b) Single-GB TFT using the calibrated energy balance model. The qualitative behaviour is similar to that observed in Walker et al. (2004), however the SOI subthreshold degradation is less severe as a consequence of the LDD structure



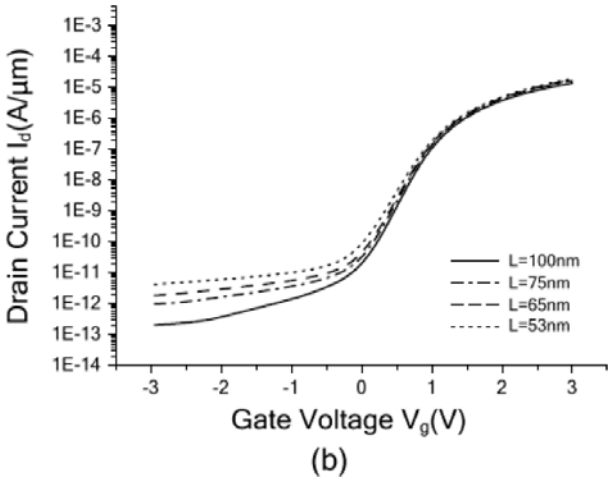
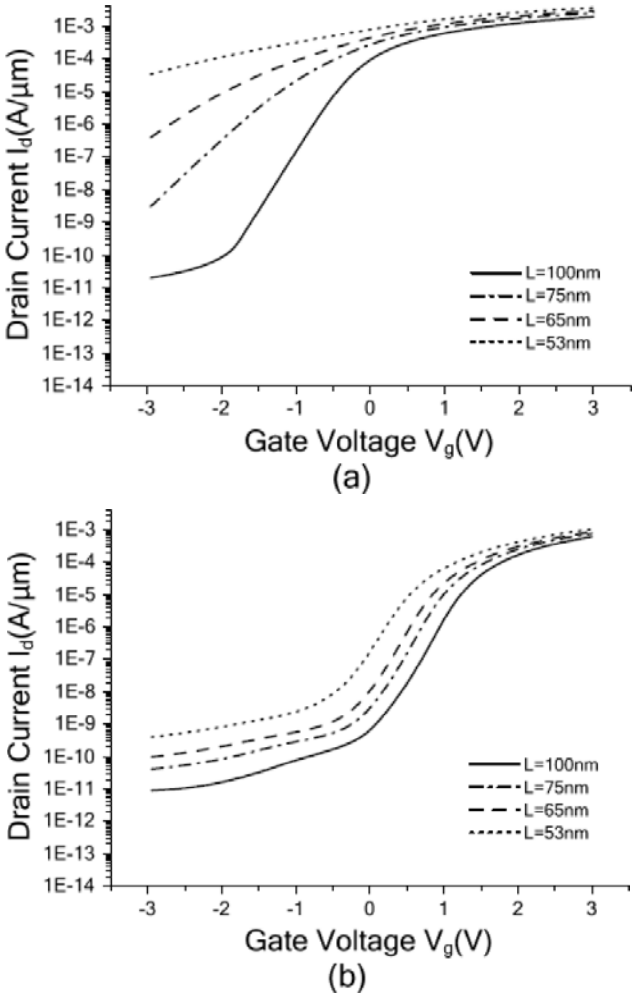


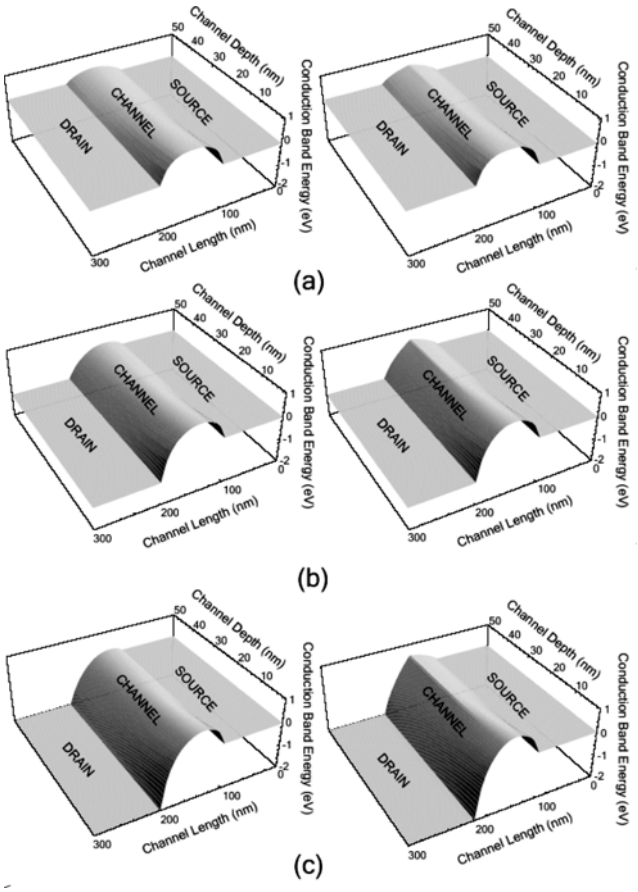
Figure 8 I_d–V_g characteristics at V_d = 1.2 V for (a) and SOI (b) Single-GB TFT using the calibrated energy balance model. The subthreshold degradation in the SOI device becomes severe at the increased drain bias whereas the single-GB TFT shows good DIBL immunity



When V_d = 0.01 V, the SOI MOSFET shows better short channel behaviour than when simulated in Walker et al.). This is because the LDD doping profile reduces the electric field at the drain edge and therefore reduces the DIBL. However, at the higher drain bias of V_d = 1.2 V, the SOI MOSFET shows poor DIBL immunity, with subthreshold slope and leakage currents becoming unacceptable as the channel length of 53 nm is approached.

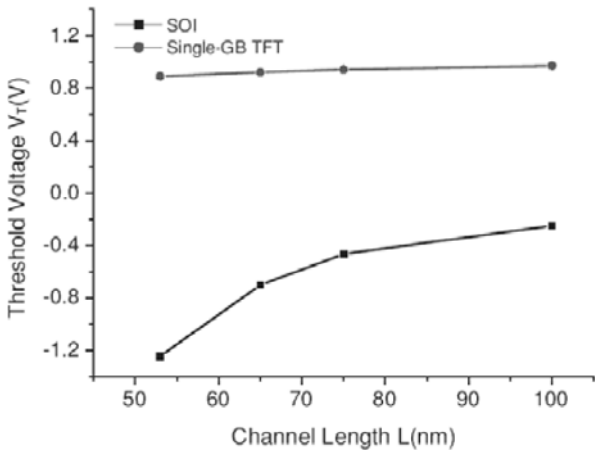
This is in contrast with the single-GB TFT which shows excellent DIBL immunity at V_d = 0.01 V and – relative to the SOI device – and improved subthreshold behaviour when V_d = 1.2 V. This result can be explained in terms of the potential barrier formed at the GB region due to the trapping of mobile carriers. The potential barrier acts to suppress the drain current in the subthreshold regime. However, when the gate voltage is increased the barrier is lowered and the device is turned on. This additional potential barrier allows suppression of the off-current where it would otherwise be unacceptably high due to drain induced barrier lowering. This is illustrated in Figure 9 which shows the conduction band potential across the single-GB TFT and an SOI equivalent when V_d = 0.01 V, 1 V and 2 V.

Figure 9 2D conduction band potentials for 100nm single-GB TFT and SOI MOSFET at V_g =–2 V for (a) V_d = 0.01 *V*, (b) V_d = 1 V and (c) 2V. The potential barrier formed around the GB provides an increased barrier to conduction even at V_d = 2 V



To summarise this behaviour we plot threshold voltage, V_T , as a function of channel length, L (Figure 10) for V_d = 0.01 V. The threshold voltage roll off is clearly larger for the SOI equivalent device. We can conclude from this, that the qualitative behaviour observed from the DD results, regarding improved subthreshold leakage and shown in Walker et al. (2004) are valid. As they remain, even when non-equilibrium transport is considered in the simulation model.

Figure 10 Threshold voltage as a function of channel length, extracted from Figure 7, for a single-GB TFT and SOI equivalent for V_d = 0.01 V



3.3 Gate induced drain leakage (GIDL)

When the transistor is biased so that it is in the 'off' state and there is a sufficiently large electric field, it is possible for carriers to tunnel from the valence band to the conduction band, thereby generating additional carriers. This is especially important when the device is under high drain bias, as then the electric field near the drain is high.

The two main mechanisms responsible are

1 Trap-assisted tunnelling.

2 Band-to-band tunnelling. In the device simulation package, ATLAS, trap-assisted tunnelling is included in the simulation model, through modifying the carrier cross sections.

They are modified by multiplying by a sum of

1 a Poole-Frenkel Coulombic barrier lowering term χ_F to take into account the increased thermal emission due to the lowered potential barrier

2 a further term to account for the field enhanced generation $\Gamma^C_{n,p}$.

This model is based on the work in Lui and Migliorato (1997). Using this model the carrier cross sections then become

$$\sigma_{PF} = \sigma\left(\chi_F + \Gamma^C_{n,p}\right) \tag{23}$$

where

$$\chi_F = \exp\left(\frac{\Delta E_{fp}}{kT_L}\right) \tag{24}$$

and

$$\Delta E_{fp} = \sqrt{\frac{q|E|}{\pi\varepsilon}} \tag{25}$$

and

$$\Gamma^C_{n,p} = \frac{\Delta E_{n,p}}{kT_L}\int_{\frac{\Delta E_{fp}}{\Delta E_n}}^{1} \exp\left(\frac{\Delta E_{n,p}}{kT_L}u - K_{n,p}u^{3/2}\right)\left[1-\left(\frac{\Delta E_{fp}}{u\Delta E_n}\right)^{5/3}\right]du \tag{26}$$

where u is the integration variable, $\Delta E_{n,p}$ is the energy range where tunnelling can occur for electrons and holes, respectively, $\Delta E_{f,p}$ is the energy by which the barrier is lowered by the Poole-Frenkel effect and $K_{n,p}$ are given by

$$K_{n,p} = \frac{4}{3}\frac{\sqrt{2m^*_e \Delta E^3_{n,p}}}{q\hbar|E|} \tag{27}$$

Band-to-band tunnelling is possible under high electric fields, where the internal band bending is severe enough to allow direct tunnelling, from the valence band to the conduction band. This is implemented in ATLAS, by using the field dependent generation term derived by Hurkx et al. (1992).

$$G_{BBT} = BB_A |E|^{BB_\Gamma} \exp\left(-\frac{BB_B}{|E|}\right) \tag{28}$$

where the parameters BB_A, BB_B and BB_G are empirical constants. The values of these parameters are typically fitted to experimental data and for our study we use the default values provided by Keeney et al. (1990) shown in Table 3.

Table 3 Band-to-Band tunnelling parameters used in Equation (28)

Parameter	BB_A	BB_B	BB_Γ
Value	9.66×10^{18} V/cm	3.07×10^{1} V/cm	2.0

To gauge the significance of the band-to-band and trap-to band tunnelling mechanisms, on the leakage current of short channel single-GB TFTs, we performed simulations of a 100 nm device. The device model was identical to that used in previously, other than being modified to include some trap states within the grains themselves. The relative importance of the grain and grain boundary traps was discussed in Armstrong et al. (1998) and we use the values suggested in this paper for the trap energy densities within the grains. These are described by the double exponential:

$$g(E) = N_{T1}\exp\left(-\frac{E_c - E}{E_1}\right) + N_{T2}\exp\left(-\frac{E_c - E}{E_2}\right) \tag{29}$$

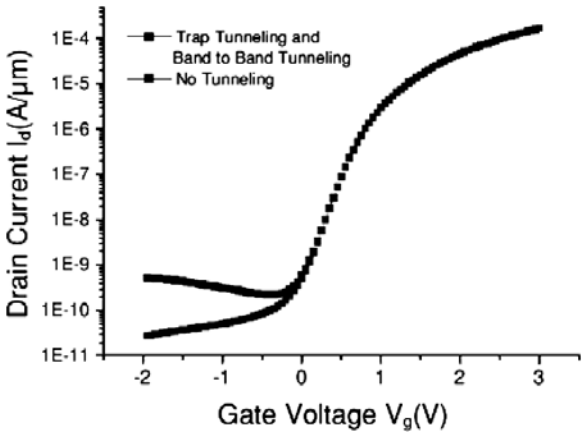
the values of N_{T1}, N_{T2}, E_1 and E_2 are given in Table 4. The same values are used for both acceptor-like and donor-like distributions.

Table 4 Parameters used for the intra-grain trap density of states in Equation (29)

Parameter	N_{T1}	N_{T2}	E_1	E_2
Value	1.3E18cm^{-3}	1E19cm^{-3}	0.2	0.035

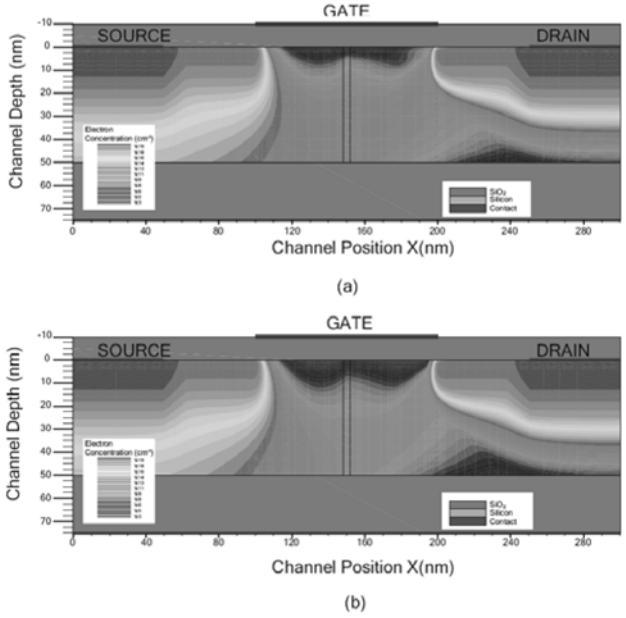
The I_d–V_s characteristics are shown in Figure 11 for V_d = 2 V with no tunnelling and both trap-to-band and band-to-band tunnelling. The results indicate some significant carrier generation the negative gate bias regime.

Figure 11 I_d–V_g characteristics with/without trap-to-band and band-to-band tunnelling models for a 100 nm single-GB TFT



The drain current shows clear field dependence, when the tunnelling mechanisms are included in the simulation model. The generation of additional carriers is illustrated in Figure 12 which shows a contour plot of the electron concentration across the device for $V_g = -2$ V, $V_d = 2$ V for (a) with and (b) without the tunnelling models. It can be seen, that there is an increased electron concentration near the drain edge (denoted by the purple shading), when band-to-band and trap-assisted tunnelling is included.

Figure 12 Electron concentration in a 100 nm single-GB TFT with intra-grain traps at $V_g = -2$ V and $V_d = 2$ V (a) with and (b) without tunnelling models



4 Conclusions

We have investigated the effect of a single-GB on the performance of decananometre-scale TFTs by using the calibrated energy balance transport model and the continuous trap state distribution at the GB. We have found that the GB potential barrier suppresses the subthreshold slope and leakage current in devices, where the DIBL effect and punchthrough currents significantly degrade device performance. We have also found that the DD model underestimates the drain current in the single-GB TFT and the velocity overshoot effect becomes significant in the short channel regime. Inclusion of trap-to-band and band-to-band tunnelling models into our simulations have shown, that the subthreshold leakage current has a significant field dependence, in the negative gate bias regime. Therefore in future work all these effects should be incorporated for a realistic simulation.

Acknowledgement

The authors would like to thank Dr. Shigeyasu Uno for his helpful discussions regarding this work.

References

Armstrong, G., Uppal, S., Brotherton, S. and Ayres, J. (1997) 'Modeling of laser-annealed polysilicon tft characteristics', *IEEE Electronic Device Letter*, Vol. 18, No. 7, pp.315–318.

Armstrong, G., Uppal, S., Brotherton, S. and Ayres, J. (1998) 'Differentiation of effects due to grain and grain boundary traps in laser annealed poly-si thin film transistors', *Japanese Journal of Applied Physics*, Vol. 37, No. 4A, pp.1721–1726.

Atlas User's Manual (2002) Silvaco International, 4701 Patrick Henry Drive, Bldg 1, Santa Clara, CA 95054.

Banerjee, K., Souri, S., Kapur, P. and Saraswat, K. (2001) '3-d ics: a novel chip design for improving deepsubmicrometer interconnect performance and systemson- chip integration', *Proceedings of the IEEE*, Vol. 89, No. 5, pp.602–633.

Chern, H.N., Lee, C.L. and Lei, T.F. (1995) 'An analytical model for the above-threshold characteristics of polysilicon thin-film transistors', *IEEE Transactions Electron Devices*, Vol. 42, No. 7, pp.1240–1246.

Chou, T-K. and Kanicki, J. (1999) 'Two-dimensional numerical simulation of solid phase-crystallized polysilicon thin-film transistor characteristics', *Japanese Journal of Applied Physics*, Vol. 38, No. 4B, pp.2251–2255.

Dimitriadis, C. and Tassis, D. (1995) 'Output characteristics of short-channel polycrystalline silicon thin-film transistors, *Journal of Applied Physics*, Vol. 77, No. 5, pp.2177–2183.

Dimitriadis, C., Tassis, D. and Economou, N. (1993) 'Determination of bulk states and interface states distributions in polyscrystalline silicon thin-film transistors', *Journal* of *Applied Physics*, Vol. 74, No. 4, pp.2919–2924.

Faughnan, B. and Ipri, A.C. (1989) 'A study of hydrogen passivation of grain boundaries in polysilicon thin-film transistors', *IEEE Transactions on Electron Devices*, Vol. 36, No. 1, pp.101–107.

Hall, R. (1952) 'Electron hole recombination in germanium', *Physics Review*, Vol. 87, p.387.

Hurkx, G., Klaassen, D. and Knuvers, M. (1992) 'A new recombination model for device simulation including tunneling', *IEEE Transaction on Electron Devices*, Vol. 39, No. 2, pp.331–338.

Ikeda, H. (2002) 'Evaluation of grain boundary trap states in polycrystalline-silicon thin-film transistors by mobility and capacitance measurements', *Journal of Applied Physics*, Vol. 91, No. 7, pp.4637–4645.

International technology roadmap for semiconductors (2003) 'Process integration', *Devices and Structures*.

Jeon, J-H., Lee, M-C., Park, K-C. and Han, M-K. (2001) 'A new polycrystalline silicon tft with a single grain boundary in the channel', *IEEE Electron Device Letter*, Vol. 22, No. 9, pp.429–431.

Kamins, T. (1998) *Polycrystalline Silicon for Integrated Circuits and Displays*, 2nd edition, Boston: Kluwer.

Keeney, S., Piccinini, F., Morelli, M. and Mathewson, A. (1990) 'Complete transient simulation of flash eeprom devices', *IEDM Technical Digest*, pp.201–204.

Kimura, M., Inoue, S., Shimoda, T. and Sameshima, T. (2001a) 'Device simulation of carrier transport through grain boundaries in lightly doped polysilicon films and dependance on dopant density', *Japanese Journal of Applied Physics*, Vol. 40, No. 9A, pp.5237–5243.

Kimura, M., Inoue, S., Shimoda, T. and Sameshima, T. (2001b) 'Device simulation of grain boundaries in lightly doped polysilicon films and analysis of dependence on defect density', *Japanese Journal of Applied Physics*, Vol. 40, No. 1, pp.49–53.

Kithahara, Y., Takagi, S. and Sano, N. (2003) 'Statistical study of subthreshold characteristics in polycrystalline silicon thin-film transistors', *Journal of Applied Physics*, Vol. 94, No. 12, pp.7789–7795.

Lui, O. and Migliorato, P. (1997) 'A new generationrecombination model for device simulation including the poole-frenkel effect and phonon-assisted tunnelling', *Solid State Electrical*, Vol. 41, No. 4, pp.575–583.

Moazzami, R. and Hu, C. (1993) 'A high-quality stacked thermal/lpcvd gate oxide technology for ulsi', *IEEE Electronic Device Letter*, Vol. 14, No. 2, p.72–73.

MOCASIM User's Manual (2002) Silvaco International, 4701 Patrick Henry Drive, Bldg 1, Santa Clara, CA 95054.

Oh, C-H. and Matsumura, M. (2001) 'A proposed single grain-boundary thin-film transistor', *IEEE Electron Device Letter*, Vol. 22, No. 1, pp.20–22.

Shockley, W. and Read, W. (1952) 'Statisitics of the recombination of holes and electrons', *Physics Review*, Vol. 87, pp.835–842.

Snowden, C. (1988) 'Semiconductor device modelling', *Materials and Devices Series 5, IEE.*

Stratton, R. (1962) 'Diffusion of hot and cold electrons in semiconductor barriers', *Physical Review*, Vol. 126, pp. 2002–2013.

Stratton, R. (1972) 'Semiconductor current-flow equations (diffusion and degeneracy)', *IEEE Transactions on Electron Devices*, Vol. 19, pp.1288–1292.

Subramanian, V., Dankoski, P., Degertekin, L., Khuri-Yakub, B. and Saraswat, K. (1997) 'Controlled two-step solid-phase crystallization for high-performance polysilicon tft's', *IEEE Electron Device Letter*, Vol. 18, No. 8, pp.378–381.

Walker, P., Mizuta, H., Uno, S., Furuta, Y. and Hasko, D. (2004) 'Improved off-current and subthreshold slope in aggressively scaled poly-si tfts with a single grain boundary in the channel', *IEEE Transactions on Electron Devices*, Vol. 51, No. 2, pp.212–219.

Yamaguchi, K. (2001) 'Modeling and characterization of polycrystalline-silicon thin-film transistors with a channel-length comparable to a grain size', *Journal of Applied Physics*, Vol. 89, No. 1, pp.590–595.

Yang, G-Y., Hur, S-H. and Han, C-H. (1999) 'A physical-based analytical turn-on model of polysilicon thin-film transistors for circuit simulation', *IEEE Transactions on Electron Devices*, Vol. 46, No. 1, pp.165–172.