Energy-balance modelling of short channel single-GB thin-film transistors

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Abstract: In this paper, we have investigated the effect of a single Grain Boundary (GB) on the performance of decananometer-scale Thin Film Transistors (TFTs) by using the calibrated energy balance transport model and a continuous trap state distribution at the GB. We have found that the GB potential barrier suppresses the subthreshold slope and leakage current in devices, where the DIBL effect and punchthrough currents significantly degrade device performance. We have also found that the drift-diffusion model underestimates the drain current in the single-GB TFT and the velocity overshoot effect becomes significant in the short channel regime. Inclusion of trap-to-band and band-to-band tunnelling models into our simulations have shown that the subthreshold leakage current has a significant field dependence in the negative gate bias regime.

Keywords: poly-silicon; grain boundary; energy-balance modelling; thin-film transistor.

Biographical notes: P.M. Walker is a Research Student at the University of Cambridge. His PhD research has been to study the potential applications of polycrystalline silicon for use in advanced submicron thin-film transistors. He received his BEng (Hons) from the University of Glasgow in 2001 and his final year dissertation concerned the fabrication and simulation of InP resonant tunnelling diodes.

Hiroshi Mizuta is a Professor of Nanoelectronics at the School of Electronics and Computer Science at the University of Southampton and a Professor at Department of Physical Electronics, Tokyo Institute of Technology. His current research interests are Si nanodots and nanowires, electron transport in Si nanostructures, ab-initio calculations of nanomaterial properties and quantum transport and their novel applications to quantum information devices and nano electromechanical devices. He has co-authored more than 200 scientific papers and filed over 50 patents. He has also co-authored books and chapters, including Physics and Applications of Resonant Tunnelling Diodes, Cambridge University Press, 1995.

1 Introduction

Polysilicon Thin-Film Transistors (TFTs) have been studied extensively in recent years for their use in flat panel active matrix displays. When polysilicon TFTs are used in AMLCD applications, the minimum feature size is typically very large (in the order of tens of microns), and therefore a large number of Grain Boundaries (GBs) are present in the channel. When modelling such devices, conventionally, reducing the average carrier mobility below the bulk-single crystal value includes the effect of the GBs. In such an analysis the discrete properties of individual GBs are not considered. More recently the polysilicon has been proposed as a device material for use in 3D VLSI circuits (Banerjee et al., 2001). For the future 3D integration of VLSI devices the channel length must be scaled to much smaller dimensions. In scaling the channel of the device down to the decananometre regime – a length and width comparable to the polysilicon grain size – it is important to understand the effects of discrete GBs on conduction (Yamaguchi, 2001).
When the poly-Si film is fabricated using Solid Phase Crystallisation (SPC) of deposited a-Si, the grain size is usually only in the order of hundreds of nanometres or less (Subramanian et al., 1997). Therefore, when using SPC films to fabricate TFTs, it follows that if we scale the transistor down to the short channel regime – that is channel length less than one micron – only a small number of GBS will be present in the device channel (Jeon et al., 2001; Oh and Matsumura, 2001). Therefore it is increasingly important to understand the effects of discrete GBS on carrier transport.

In our previous work (Walker et al., 2004) we modelled a TFT with a single grain boundary located at the centre of the channel and oriented perpendicular to the direction of current flow. We showed that improvements in the subthreshold slope and leakage current were possible in short channel single-GB TFTs, relative to their SOI equivalents.

To perform the simulation we used a 2D drift diffusion model, with a localised trap model where the traps were located only at the GB region. Generation and recombination processes from the traps were simulated using Shockley-Read-Hall statistics and the traps were assumed to be mono-energetic and located close to the middle of the forbidden energy gap.

In this work we seek to improve the realism of the simulation model used in Walker et al. (2004) and to thereby validate it’s conclusions. There are two key improvements that can be made to the simulation model.

Firstly, instead of using mono-energetic traps, we include distribution of traps across the energy band gap, where the distribution is based on experimental measurements.

Secondly, we can use the Energy-Balance (EB) model instead of the conventional Drift-Diffusion (DD) model. This is especially important as the channel lengths are scaled into the decananometer regime because of hot carrier effects.

Finally, we can include additional generation and recombination effects due to the tunnelling of carriers directly from the valence band to the conduction band or via the trap states in high electric fields. This is important as in the high electric fields found in a short channel device additional current due to tunnelling can be significant.

Currently, we do not model quantum mechanical effects such as phonon limited electron mobility, reduction in inversion layer charge or direct tunnelling from the source to the drain.

## 2 Simulation model

### 2.1 EB model

Previously, we used the basic DD formulation of the semiconductor device equations. These assume that the carrier temperatures are in equilibrium with the surrounding crystal lattice. Thus, not taking into account the possibility of non-equilibrium transport, that can occur when strong electric fields are present in short channel devices. The high electric fields can cause substantial heating of carriers, resulting in carrier energies, which far exceed those of equilibrium. The velocity overshoot effect occurs when carriers in large electric fields are accelerated to velocities larger than the equilibrium saturation limit. Not including this effect can lead to underestimation of the drain currents in MOSFET simulations. It has been estimated that these effects can become significant in MOSFETs with channel lengths less than ≈100 nm (Snowden, 1988). Therefore, for accurate simulation of devices in this regime, an extended DD model derived from the higher order moments of the Boltzmann equation is often used; this incorporates, carrier temperature/energy, as a further transport parameter. One model using this approach is the energy balance model (Stratton, 1962, 1972) and it is incorporated into the (ATLAS User’s Manual, 2002) device simulation package, which we use for all the simulations presented in this paper.

The energy balance model consists of a set of six coupled partial differential equations, which are for energy balance, current density $\overline{J_{n,p}}$, and energy flux $\overline{S_{n,p}}$ for both holes and electrons, respectively.

Assuming Boltzmann statistics, then for electrons these consist of:

$$\nabla \overline{S_{n}} = \frac{1}{q} \overline{J_{n}} E - \frac{3}{2} \frac{k_{B}}{\tau_{n}} - \overline{W_{n}}$$

(1)

$$\overline{J_{n}} = qD_{n} \nabla n - q\mu_{n} n \nabla \phi + qnD_{n}^{T} \nabla T_{n}$$

(2)

$$\overline{S_{n}} = -K_{n} \nabla T_{n} - \left( \frac{3}{2} \frac{k_{B}}{q} \right) \overline{J_{n}} T_{n}$$

(3)

and for holes:

$$\nabla \overline{S_{p}} = \frac{1}{q} \overline{J_{p}} E - \frac{3}{2} \frac{k_{B}}{\tau_{p}} - \overline{W_{p}}$$

(4)

$$\overline{J_{p}} = qD_{p} \nabla p - q\mu_{p} p \nabla \phi + qnD_{p}^{T} \nabla T_{p}$$

(5)

$$\overline{S_{p}} = -K_{p} \nabla T_{p} - \left( \frac{3}{2} \frac{k_{B}}{q} \right) \overline{J_{p}} T_{p}$$

(6)

where two independent variables $T_{n}$ and $T_{p}$ have been used for the electron and hole temperatures, respectively, $T_{L}$ is the lattice temperature and $T_{n}^{e}$, $T_{p}^{e}$ are the energy relaxation times for electrons and holes, respectively. The energy flux densities for electrons and holes are given as $\overline{S_{n}}$ and $\overline{S_{p}}$. $D_{n}$ and $D_{p}$ are the temperature dependent diffusivities given by

$$D_{n} = \frac{\mu_{n} k_{B} T_{n}}{q}$$

(7)

$$D_{p} = \frac{\mu_{p} k_{B} T_{p}}{q}$$

(8)

$K_{n}$ and $K_{p}$ are the thermal conductivities where all for electrons and holes, respectively given by

$$K_{n} = qn\mu_{n} \left( \frac{3}{2} \frac{k_{B}}{q} \right) T_{n}$$

(9)
\[ K_p = q \rho_p \left( \frac{3}{2} \frac{k^2}{q^2} \right) T_p \]  

(10)

\[ W_n = \frac{3}{2} \frac{k(T_n - T_i)}{\tau_{n}} + \frac{3}{2} k T_p R_{oh} \]  

(11)

\[ W_p = \frac{3}{2} \frac{k(T_p - T_i)}{\tau_{p}} + \frac{3}{2} k T_p R_{oh} \]  

(12)

The energy relaxation time governs the magnitude of the non-stationary transport effects such as velocity overshoot, therefore it is a critical parameter in the energy balance model. In the classical DD model, this time is assumed to be zero and the energy density loss rates can be expressed as:

\[ W_n = \frac{3}{2} \frac{k(T_n - T_i)}{\tau_{n}} + \frac{3}{2} k T_p R_{oh} \]  

(11)

2.2 Calibration of energy relaxation times using Monte-Carlo simulation

The energy relaxation time \( \tau_{n/e} \) for electrons and holes is a critical parameter in the energy balance scheme of equations. It is a measure of the amount of time needed for the carrier energy to reach equilibrium with the electric field. The larger the relaxation time the greater the magnitude of the non-stationary effects. In the classical DD model, this time is assumed to be zero and the maximum carrier velocity is given by the velocity saturation limit. In the energy balance regime the velocity can overshoot this value before returning to the equilibrium level after a finite time; this is the energy relaxation time.

The default model in ATLAS assumes a constant relaxation time for both holes and electrons of 0.25 ps. The value of the relaxation time is controversial, as it is not directly measurable and incorrect values can lead to non-physical behaviour in the simulations. The best approach, to determine suitable values for the carrier relaxation times, is to use bulk Monte-Carlo simulations to evaluate the ensemble average value. We use the commercial Monte-Carlo simulator ‘MOCASIM’ (MOCASIM User’s Manual, 2002). In this simulation, a finite number of electrons are generated in equilibrium at a specific field, doping and temperature. The system is allowed to evolve from an initial distribution and how it changes with time is evaluated by calculating the scattering of the carriers at each time step. The allowed scattering mechanisms are specified in the simulation input file and the process continues until the carrier distribution converges to a steady state. It is at this point that the transport parameters can be extracted, by taking the average of the ensemble.

The parameters used in our simulation are summarised in Table 1. In the Monte-Carlo simulations the silicon is assumed to be intrinsic, therefore no doping dependency is currently incorporated into the model. The extracted relaxation time for electrons against carrier energy is plotted in Figure 1, along with a curve fitted using an arbitrary function. The carrier energy dependence of the energy relaxation time is then incorporated into the device simulations by modifying the energy balance model to use the function of the curve fit to evaluate the relaxation time for each mesh node. It was found that using our energy dependent relaxation time also helped ATLAS converge to a solution when using the EB model.

<table>
<thead>
<tr>
<th>Simulation parameter</th>
<th>Parameter value</th>
</tr>
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<tbody>
<tr>
<td>Number of carriers</td>
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</tr>
<tr>
<td>Doping density</td>
<td>( 1 \times 10^{11} ) cm(^{-3} )</td>
</tr>
<tr>
<td>Number of time steps</td>
<td>20,000</td>
</tr>
<tr>
<td>Time step</td>
<td>( 1 \times 10^{-15} ) s</td>
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</table>

<table>
<thead>
<tr>
<th>Scattering mechanism</th>
<th>Intervally phonon energy</th>
<th>Deformation potential</th>
<th>Number of valleys</th>
</tr>
</thead>
<tbody>
<tr>
<td>Acoustic phonon</td>
<td>N/A</td>
<td>9.5 V/cm</td>
<td>N/A</td>
</tr>
<tr>
<td>scattering</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Intervally phonon</td>
<td>0.01206 eV,</td>
<td>0.50 \times 10^{8} V/cm</td>
<td>2</td>
</tr>
<tr>
<td>scattering</td>
<td>0.01810 eV,</td>
<td>0.80 \times 10^{8} V/cm</td>
<td>2</td>
</tr>
<tr>
<td>(X-&gt;X)</td>
<td>0.06032 eV,</td>
<td>3.00 \times 10^{8} V/cm</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>0.01810 eV,</td>
<td>0.15 \times 10^{8} V/cm</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>0.04309 eV,</td>
<td>2.50 \times 10^{8} V/cm</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>0.05429 eV,</td>
<td>4.00 \times 10^{8} V/cm</td>
<td>2</td>
</tr>
<tr>
<td>Ionised impurity</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>scattering</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 1  Energy relaxation time \( \tau \) plotted against electron energy for intrinsic silicon. An arbitrary function was fitted to the data points supplied by the Monte Carlo simulation to approximate the temperature dependence of the relaxation times in the energy balance model.

2.3 Modelling of grain boundary trap states

To model the inclusion of trap states in the forbidden gap the space charge term on the right-hand side of Poisson’s equation is modified by including an additional charge term \( Q_T \) representing trapped charge. This is given by
\[-\rho = q\left( p - n + N_d^* - N_a^* \right) + Q_t \quad (13)\]

\[Q_t = q\left( p_r - n_r \right) \quad (14)\]

where \( N_d^* \) and \( N_a^* \) are the ionised donor and acceptor concentrations, respectively and \( p_r \) and \( n_r \) are the trapped hole and electron concentrations, respectively. We assume that the trap states consist of both donor- and acceptor-like states distributed across the forbidden energy gap, where the donor-like states act as hole traps and the acceptor-like traps act as electron traps. Therefore the total density of states is given by

\[ g(E) = g_d(E) + g_a(E) \quad (15)\]

where \( g_d(E) \) is the total density of donor-like trap states and \( g_a(E) \) is the total density of acceptor-trap states. To calculate the trapped charge we perform a numerical integration of the product of the trap density and its occupation probability over the forbidden energy gap. This gives

\[ n_t = \int_{E_i}^{E_c} g_d(E)f_d(E,n,p)dE \quad (16)\]

\[ p_t = \int_{E_i}^{E_c} g_a(E)f_a(E,n,p)dE \quad (17)\]

for trapped electrons and holes, respectively, where \( f_d \) and \( f_a \) are the occupation probability for acceptor-like and donor-like traps.

The occupation probabilities are then given by

\[ f_d = \frac{v_e\sigma_{ae}(n + n_i) + v_h\sigma_{ah}(p + p_i)}{v_e\sigma_{ae}(n + n) + v_h\sigma_{ah}(p + p)} \quad (18)\]

\[ f_D = \frac{v_e\sigma_{ae}(n + n_i) + v_h\sigma_{ah}(p + p_i)}{v_e\sigma_{ae}(n + n) + v_h\sigma_{ah}(p + p)} \quad (19)\]

where \( \sigma_{ae}, \sigma_{ah}, \sigma_{ae}, \sigma_{ah} \) are the electron and hole capture cross sections for acceptor-like and donor-like traps, respectively. The effective electron and hole concentrations \( n_e \) and \( p_i \) are defined as

\[ n_e = n_i \exp \left[ \frac{E - E_i}{kT} \right] \quad (20)\]

\[ p_i = n_i \exp \left[ \frac{E - E_c}{kT} \right] \quad (21)\]

where \( n_i \) is the intrinsic carrier concentration, \( E \) is the trap energy level, \( E_i \) is the intrinsic fermi level and \( T \) is the lattice temperature.

The Shockley–Read–Hall recombination/generation rate (Hall, 1952; Shockley and Read, 1952) per unit time is modified to include the multiple trap levels and is given by

\[ U_{n,p} = \int_{E_i}^{E_c} \left( \frac{v_ev_p\sigma_{ae}\sigma_{ah}(np-n_i^2)g_d(E)}{v_e\sigma_{ae}(n + n_i) + v_h\sigma_{ah}(p + p_i)} \right. \]

\[ + \left. \frac{v_ev_p\sigma_{ae}\sigma_{ah}(np-n_i^2)g_a(E)}{v_e\sigma_{ae}(n + n_i) + v_h\sigma_{ah}(p + p_i)} \right) \quad (22)\]

2.4 Trap state distribution model

As discussed in the introduction, in our previous simulation study (Walker et al., 2004), we assumed that the trap states were mono-energetic. That is, they existed at a fixed point in the energy band gap. Experiment studies have shown that this model is unrealistic and that the traps are in fact spread over the band gap with acceptor-like traps closer to the conduction band and donor-like traps closer to the valence band. The device simulation package ATLAS allows us to define a density of defect states as a combination of four bands. Two tail bands are specified that contain large numbers of defect states at the conduction band (acceptor-like traps) and valence band (donor-like traps) edges, respectively. These both decay rapidly as we move towards the centre of the forbidden energy gap. In addition two deep level bands are defined (acceptor and donor-like) which are modelled using a gaussian distribution with its peak close to the middle of the forbidden energy gap.

However, many different trap density distributions have been proposed to describe the position and density of the traps within the polysilicon band gap. These have consisted of single energy level models (Walker et al., 2004; Yang et al., 1999), models with single (Chern et al., 1995) or double (Armstrong et al., 1997, 1998; Chou and Kanicki, 1999) exponential tail states, gaussian shaped distributions (Kamins, 1998; Kimura et al., 2001a,b) or both (Faughnan and Ipri, 1989; Ikeda, 2002). It has been suggested that the tail states dominate the above threshold behaviour while the mid-gap states primarily effect the subthreshold behaviour (Armstrong et al., 1997; Chern et al., 1995). In this study we are concerned with the both the subthreshold region and the above threshold region. So to ensure a realistic model we chose to include both mid-gap and tail states. The trap density distributions used in our simulation study are plotted in Figure 2 as a function of energy.

**Figure 2** The distribution of the acceptor and donor-like trap states across the forbidden energy gap that are used in our simulation study

As it is widely accepted that the trap density distribution contains exponential band tails at the valence and conduction band edges, when deciding on a suitable distribution the main qualitative choice is whether to include the mid-gap states as additional exponential terms
such as in Armstrong et al. (1997, 1998) and Chou and Kanicki (1999) or as gaussian terms as used in Dimitriadis et al. (1993) Dimitriadis and Tassis (1995) and Ikeda (2002). We choose to use gaussian terms; the reason being that the papers dealing with SPC films suggest a peak in trap states near the mid-gap and it is SPC films that we are considering in this work. The values chosen are in the range suggested in Dimitriadis et al. (1993) and are given in Table 2.

### Table 2

<table>
<thead>
<tr>
<th>Device Parameter</th>
<th>Symbol/units</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>$L$ (nm)</td>
<td>400</td>
</tr>
<tr>
<td>Channel width</td>
<td>$L$ (nm)</td>
<td>1000</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>$t_{ox}$ (nm)</td>
<td>10</td>
</tr>
<tr>
<td>Polysilicon thickness</td>
<td>$t_p$ (nm)</td>
<td>25/50</td>
</tr>
<tr>
<td>Buried oxide thickness</td>
<td>$t_{box}$ (nm)</td>
<td>25</td>
</tr>
<tr>
<td>Source and drain dopant density</td>
<td>$n^+$ (cm$^{-3}$)</td>
<td>$1 \times 10^{21}$</td>
</tr>
<tr>
<td>Width of grain boundary</td>
<td>$W_{gb}$ (nm)</td>
<td>4</td>
</tr>
<tr>
<td>Capture cross section of electrons in acceptor-like states</td>
<td>$\sigma_{ae}$ (cm$^2$)</td>
<td>$1 \times 10^{-16}$</td>
</tr>
<tr>
<td>Capture cross section of holes in acceptor-like states</td>
<td>$\sigma_{ah}$ (cm$^2$)</td>
<td>$1 \times 10^{-14}$</td>
</tr>
<tr>
<td>Capture cross section of electrons in donor-like states</td>
<td>$\sigma_{de}$ (cm$^2$)</td>
<td>$1 \times 10^{-14}$</td>
</tr>
<tr>
<td>Capture cross section of holes in donor-like states</td>
<td>$\sigma_{dh}$ (cm$^2$)</td>
<td>$1 \times 10^{-14}$</td>
</tr>
<tr>
<td>Density of acceptor-tail states</td>
<td>$N_{T}$ (cm$^{-3}$)</td>
<td>$1 \times 10^{16}$</td>
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<tr>
<td>Density of donor-tail states</td>
<td>$N_{D}$ (cm$^{-3}$)</td>
<td>$1 \times 10^{21}$</td>
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<td>Density of acceptor-gaussian states</td>
<td>$N_{GA}$ (cm$^{-3}$)</td>
<td>$4 \times 10^{20}$</td>
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<td>$W_{TA}$ (eV)</td>
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<td>Decay energy for donor-tail states</td>
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<td>$W_{GA}$ (eV)</td>
<td>0.1</td>
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<tr>
<td>Decay energy for donor-gaussian states</td>
<td>$W_{GD}$ (eV)</td>
<td>0.1</td>
</tr>
<tr>
<td>Energy of gaussian for acceptor-states</td>
<td>$E_{GA}$ (eV)</td>
<td>0.51</td>
</tr>
<tr>
<td>Energy of gaussian for donor-states</td>
<td>$E_{GD}$ (eV)</td>
<td>0.51</td>
</tr>
</tbody>
</table>

#### 2.5 Device structure

Figure 3 shows the basic device structure we used for the device modelling. In this simple structure we assumed a thin polysilicon layer of $t_d = 50$ nm, this is to facilitate easy comparison with the results for subthreshold behaviour, presented in Walker et al. (2004). A gate oxide of 10 nm is chosen, which we estimate is near limit of the thickness that is possible in polysilicon, due to surface roughness at the oxide-polysilicon interface (Moazzami and Hu, 1993). The source and drain regions are heavily doped $n$-type material, with a doping density of $1 \times 10^{21}$cm$^{-3}$, while the channel region is intrinsic. In our model there are no trap states located in the grain regions, only in the grain boundary region. In previous simulation studies the GB width has been assumed to be within 1–5 nm, in our simulation it is 4 nm in width which is within this range (Kithahara et al., 2003; Yamaguchi, 2001).

![Figure 3](image)

We choose to limit the maximum channel length used in this study to $L = 100$ nm. This is because 100 nm is close to the limit where the DD model is thought to become inaccurate and is of a magnitude in the order of the size of grains that are typically obtained by SPC of deposited a-Si.

The grains of the polysilicon were assumed to be columnar. In the channel of the modelled device only a single GB was included and oriented so it was perpendicular to the semiconductor interface. The lightly doped source and drain are designed to reduce the electric field at their boundary with the channel and therefore facilitate better immunity to short channel effects such as DIBL. The same structure is used when simulating SOI devices for comparison, with the obvious exception of the traps at the GB region.

#### 3 Simulation results

##### 3.1 Comparison of DD and EB model

The devices simulated had channel lengths of 100 nm and the device structure is as shown in Figure 3. The bias conditions of the simulation were set at $V_g = 0.01$ and 1.2 V, respectively, the latter value is chosen as this is the power supply voltage specified for low standby power transistor operation in the ITRS (2003).

A comparison of the $I_d – V_g$ characteristics when using the DD model and the calibrated EB model is shown in Figure 4. We observe that the drain currents predicted using the EB model are higher than those when using the DD model. This can be explained by considering the velocity overshoot effect. As previously discussed velocity overshoot is the consequence of the finite time needed for the energy of the carriers to return to their equilibrium values. The velocity overshoot effect is especially...
important at high drain bias, as the electric field strength is higher, and therefore non-equilibrium transport effects are significant. In our results, when $V_d = 0.01\, \text{V}$ the difference in drain currents is smaller in comparison to the difference when $V_d = 1.2\, \text{V}$. If we then compare the plots of electron velocity against channel position at 1nm from the semiconductor/oxide interface (Figure 5), we can clearly see that the carrier velocity is much higher, when using the EB model.

**Figure 4** An overlay of the $I_d-V_g$ characteristics at $V_d = 0.01\, \text{V}$ and $1.2\, \text{V}$ for a 100 nm single-GB TFT. A comparison is made between the results from the DD model and the calibrated EB model

![DD Model vs Calibrated EB Model](image)

**Figure 5** A comparison of the electron velocity in the channel of the single-GB TFT ($V_d = 1.2\, \text{V}$ and $V_g = 3\, \text{V}$) when using the DD or calibrated EB model. The max electron velocity is higher when using the EB model due to the velocity overshoot effect

![Electron Velocity Plot](image)

This is as a direct consequence of the velocity overshoot effect and this is the reason for the increased drain current. The $I_d-V_g$ characteristics are shown in Figure 6. These provide further clear illustration of the larger drain currents that result when using the EB model.

**3.2 Validation of improved subthreshold behaviour**

We then investigated if the trend towards improved subthreshold behaviour compared to the SOI equivalent is still found when using the EB model. Both single-GB TFT and equivalent SOI devices were simulated, using the same structure as before and with channel lengths of 100 nm, 75 nm, 65 nm and 53 nm. Convergence time for simulating single-GB TFTs was found about 3–4 times as long as that for SOI devices as a result of including the modelling of the GB traps. Default convergence criteria parameters set in ATLAS were adopted, that are enough for most purposes. The $I_d-V_g$ characteristics of the simulated devices are shown in Figures 7 and 8, for $V_g = 0.01\, \text{V}$ and $1.2\, \text{V}$, respectively.

**Figure 6** An overlay of the $I_d-V_g$ characteristics at $V_g = 1\, \text{V}$, 2 $\text{V}$, 3 $\text{V}$, 4 $\text{V}$ for a 100nm single-GB TFT. Comparison between the results from the DD model and the calibrated EB model show that larger drain currents result when the EB model is used

![DD Model vs Calibrated EB Model](image)

**Figure 7** $I_d-V_g$ characteristics at $V_g = 0.01\, \text{V}$ for (a) SOI and (b) Single-GB TFT using the calibrated energy balance model. The qualitative behaviour is similar to that observed in Walker et al. (2004), however the SOI subthreshold degradation is less severe as a consequence of the LDD structure

![SOI vs Single-GB TFT Comparison](image)
Figure 8  
$I_d$-$V_g$ characteristics at $V_d = 1.2$ V for (a) and SOI (b) Single-GB TFT using the calibrated energy balance model. The subthreshold degradation in the SOI device becomes severe at the increased drain bias whereas the single-GB TFT shows good DIBL immunity.

When $V_d = 0.01$ V, the SOI MOSFET shows better short channel behaviour than when simulated in Walker et al.). This is because the LDD doping profile reduces the electric field at the drain edge and therefore reduces the DIBL. However, at the higher drain bias of $V_d = 1.2$ V, the SOI MOSFET shows poor DIBL immunity, with subthreshold slope and leakage currents becoming unacceptable as the channel length of 53 nm is approached.

This is in contrast with the single-GB TFT which shows excellent DIBL immunity at $V_d = 0.01$ V and – relative to the SOI device – and improved subthreshold behaviour when $V_d = 1.2$ V. This result can be explained in terms of the potential barrier formed at the GB region due to the trapping of mobile carriers. The potential barrier acts to suppress the drain current in the subthreshold regime. However, when the gate voltage is increased the barrier is lowered and the device is turned on. This additional potential barrier allows suppression of the off-current where it would otherwise be unacceptably high due to drain induced barrier lowering. This is illustrated in Figure 9 which shows the conduction band potential across the single-GB TFT and an SOI equivalent when $V_d = 0.01$ V, 1 V and 2 V.

To summarise this behaviour we plot threshold voltage, $V_T$, as a function of channel length, L (Figure 10) for $V_d = 0.01$ V. The threshold voltage roll off is clearly larger for the SOI equivalent device. We can conclude from this, that the qualitative behaviour observed from the DD results, regarding improved subthreshold leakage and shown in Walker et al. (2004) are valid. As they remain, even when non-equilibrium transport is considered in the simulation model.

Figure 9  
2D conduction band potentials for 100nm single-GB TFT and SOI MOSFET at $V_g = -2$ V for (a) $V_d = 0.01$ V, (b) $V_d = 1$ V and (c) 2 V. The potential barrier formed around the GB provides an increased barrier to conduction even at $V_d = 2$ V

Figure 10  
Threshold voltage as a function of channel length, extracted from Figure 7, for a single-GB TFT and SOI equivalent for $V_d = 0.01$ V
3.3 Gate induced drain leakage (GIDL)

When the transistor is biased so that it is in the ‘off’ state and there is a sufficiently large electric field, it is possible for carriers to tunnel from the valence band to the conduction band, thereby generating additional carriers. This is especially important when the device is under high drain bias, as then the electric field near the drain is high.

The two main mechanisms responsible are:

1. Trap-assisted tunnelling.
2. Band-to-band tunnelling. In the device simulation package, ATLAS, trap-assisted tunnelling is included in the simulation model, through modifying the carrier cross sections.

They are modified by multiplying by a sum of:

1. a Poole-Frenkel Coulombic barrier lowering term \( \chi_F \) to take into account the increased thermal emission due to the lowered potential barrier.
2. a further term to account for the field enhanced generation \( \Gamma_{n,p} \).

This model is based on the work in Lui and Migliorato (1997). Using this model the carrier cross sections then become

\[
\sigma_{sp} = \sigma \left( \chi_F + \Gamma_{n,p} \right)
\]

where

\[
\chi_F = \exp \left( \frac{\Delta E_{p}}{kT_L} \right)
\]

and

\[
\Delta E_{p} = \sqrt{\frac{qE}{\pi e}}
\]

and

\[
\Gamma_{n,p} = \frac{\Delta E_{n,p}}{kT_L} \int_{E_n}^{E_p} \exp \left( \frac{\Delta E_{n,p}}{kT_L} u - K_{n,p} u^{3/2} \right) \left[ 1 - \left( \frac{\Delta E_{n,p}}{u} \right)^{3/2} \right] du
\]

where \( u \) is the integration variable, \( \Delta E_{n,p} \) is the energy range where tunnelling can occur for electrons and holes, respectively, \( \Delta E_{p} \) is the energy by which the barrier is lowered by the Poole-Frenkel effect and \( K_{n,p} \) are given by

\[
K_{n,p} = \frac{4}{3} \sqrt{\frac{2m^* \Delta E_{n,p}^3}{q\hbar |E|}}
\]

Band-to-band tunnelling is possible under high electric fields, where the internal band bending is severe enough to allow direct tunnelling, from the valence band to the conduction band. This is implemented in ATLAS, by using the field dependent generation term derived by Hurkx et al. (1992).

The \( I_d-V_g \) characteristics are shown in Figure 11 for \( V_d = 2 \) V with no tunnelling and both trap-to-band and band-to-band tunnelling. The results indicate some significant carrier generation the negative gate bias regime.
The drain current shows clear field dependence, when the tunnelling mechanisms are included in the simulation model. The generation of additional carriers is illustrated in Figure 12 which shows a contour plot of the electron concentration across the device for $V_g = -2$ V, $V_d = 2$ V for (a) with and (b) without the tunnelling models. It can be seen, that there is an increased electron concentration near the drain edge (denoted by the purple shading), when band-to-band and trap-assisted tunnelling is included.

**Figure 12** Electron concentration in a 100 nm single-GB TFT with intra-grain traps at $V_g = -2$ V and $V_d = 2$ V (a) with and (b) without tunnelling models

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### 4 Conclusions

We have investigated the effect of a single-GB on the performance of decanometre-scale TFTs by using the calibrated energy balance transport model and the continuous trap state distribution at the GB. We have found that the GB potential barrier suppresses the subthreshold slope and leakage current in devices, where the DIBL effect and punchthrough currents significantly degrade device performance. We have also found that the DD model underestimates the drain current in the single-GB TFT and the velocity overshoot effect becomes significant in the short channel regime. Inclusion of trap-to-band and band-to-band tunnelling models into our simulations have shown, that the subthreshold leakage current has a significant field dependence, in the negative gate bias regime. Therefore in future work all these effects should be incorporated for a realistic simulation.

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### References


