

Anomalous suppression of single-electron tunnelling observed for Si nanobridge transistors with a suspended quantum dot cavity

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Introduction

Recent advance on fabricating silicon nano electromechanical systems (NEMS) has enabled us to study single-electron tunnelling through nanometer-scale suspended structures with restrained coupling to the environment [1]. In particular, a suspended quantum dot cavity structure built on a Si nanobridge provides an ideal system to explore the interaction of single electrons with tailored phonon spectrum in the cavity which is acoustically isolated from the Si substrate. Such a system has recently become of great interest in terms of studying physics of decoherence mechanisms for quantum bits and also revealing ultimate energy dissipation process in Si nanostructures. We also expect for such systems a variety of new electromechanical phenomena to emerge, which include formation of phononic bandgaps & phonon confinement [2], a reduction of electron-phonon interaction [3][4], phonon blockade [5], metal-insulator transition, quantization of nanomechanical motion [6], and a strong coupling of nanomechanical and electron motions [7]. These phenomena may lead to novel functional Si nano information devices [8] which are not achieved by using the conventional bulk Si CMOS technologies.

Here, we report on anomalous suppression of single-electron tunnelling observed for a low source-to-drain region. These characteristics are attributable to the enhanced interaction between tunneling electrons and cavity phonons.

Suppression of single-electron tunnelling

We fabricated a quantum dot cavity integrated on a nanobridge by combining EB-lithography and thermal oxidation [1]. We first patterned wire structures on a SOI wafer and etch the wire in the wedged shape by using EB-lithography and ECR-RIE. SiO₂ under the wire was etched out by using liquid HF and a suspended nanobridge was formed. Finally, we thermally oxidized the nanobridge to make potential barriers at the narrow area and decrease the quantum dot size.

Figure 1 (a) shows a single quantum dot cavity built on a nanobridge. We measured electrical characteristics for the device with the nanobridge of about 400 nm in length, 90 nm in width and 40 nm in thickness.

Figure 2 shows single electron transport charac-

teristics for the device measured at 4.2 K. We can clearly identify Coulomb diamonds, but a half of the diamonds are found offset. and conductance is therefore suppressed for a finite range of source-to-drain bias voltage. The measured diamonds, which are marked by solid lines, shift both in the directions of the source-to-drain bias voltage and also gate voltage axes. This is in contrast to the conventional shape of the diamonds which are shown by using dotted lines. This phenomenon cannot be explained by assuming the conventional single electron transistor. (Even if we had extra charging islands in addition to the quantum dot, the diamonds would shift only in the direction of the source-to-drain voltage axis.)

Discussion on the tunneling current suppression

Phonon blockade is the one of the possible origins of the phenomenon [5]. Phonon spectra in quantum dot cavities can be quite different from those for bulk materials and may exhibit van Hove singularities in the density of states as reported in [9]. As a result of this, electron-phonon coupling may be enhanced in these suspended phonon cavity. Tunneling single-electron may induce mechanical excitation of the suspended cavity. The electron is then inelastically scattered by the cavity phonons and cannot tunnel out from the cavity unless the source-to-drain voltage exceeds the cavity phonon energy. This is the phonon blockade of single-electron tunneling. $\delta V_{ds} = \epsilon_0/e$ and $\delta V_{gs} = \epsilon_0 C_{\Sigma}/2eC_g$ are needed in order to lift the blockade. Here, ϵ_0 is energy of a phonon localized in the cavity, e is the electron charge, C_g is a gate capacitance and C_{Σ} is a total capacitance. The lowest van Hove singularity for a cavity thickness of $z = 40$ nm is estimated at $\epsilon_0/e = \hbar\Omega_{ph} \sim 3\hbar c_L/z = 414 \mu\text{eV}$ [5].

The temperature of 4.2 K is equal to 362 μeV . It is possible to observe the phonon blockade at 4.2 K because the thermal energy is smaller than $\hbar\Omega_{ph}$.

In our results, δV_{ds} is about 8 mV. However, we have considerable potential drops along the nanobridge channel and a net voltage across the cavity is expected to be much smaller than the bare source-to-drain voltage. To have a rough estimate of the net voltage applied across the cavity, we performed the 3D drift-diffusion simulation and calculated the potential distribution along the nanobridge

channel at room temperature. When 10 mV was applied at the both side of the nanobridge, the effective voltage drop across the cavity was found to be about 3.5 mV as shown in fig. 3 and fig. 4. We may expect that the net voltage drop is even smaller in reality due to the contact resistances between Si and Al pad, surface roughness of the nanobridge and very low temperatures. As a result of these, it is likely that the effective voltage is less than 1 mV, approaching our theoretical estimate of $\hbar\Omega_{ph}$.

Double quantum dot

We also perform electrical measurements for the double quantum dot cavity embedded in a nanobridge such as shown in fig. 1 (b). We will present these results on the day of the workshop.

References

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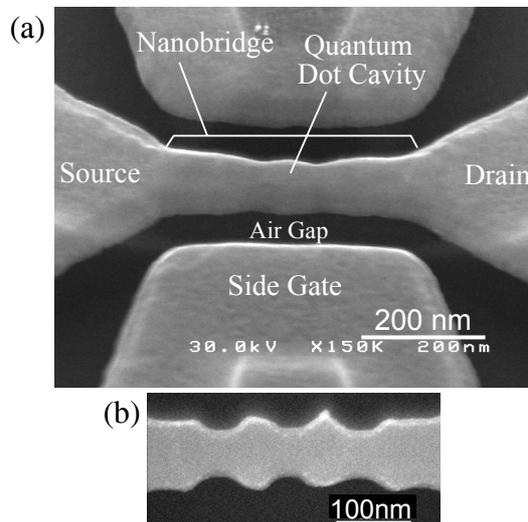


Fig. 1: SEM image of a quantum dot cavity built on a nanobridge. (a) A single quantum dot device. This image was taken obliquely and shows a 3D structure of the suspended nanobridge. (b) Top view of a double quantum dot device.

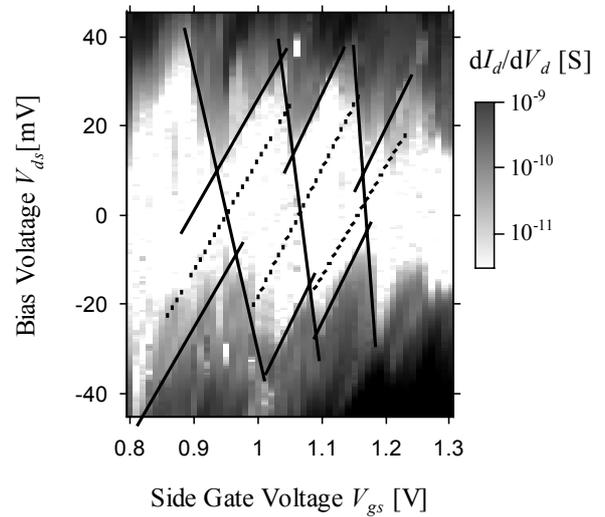


Fig. 2: Single electron transport characteristics in the quantum dot cavity on the nanobridge.

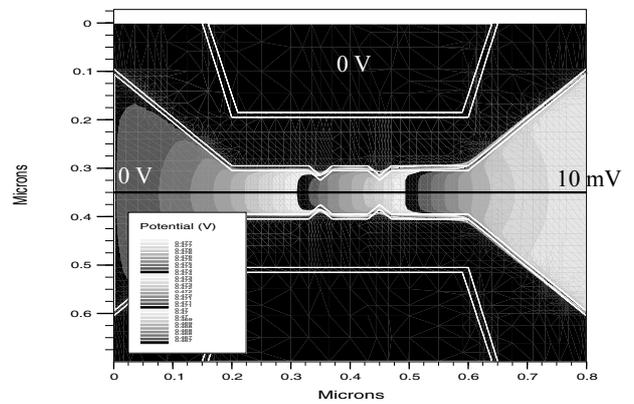


Fig. 3: Potential distribution in a nanobridge. The size of the nanobridge is 400 nm in length, 90 nm in width and 40 nm in thickness. 10 nm thick thermal oxidized layer covers the nanobridge. We put 0 V on source voltage, 10 mV on drain voltage and 0 V on side gate voltage.

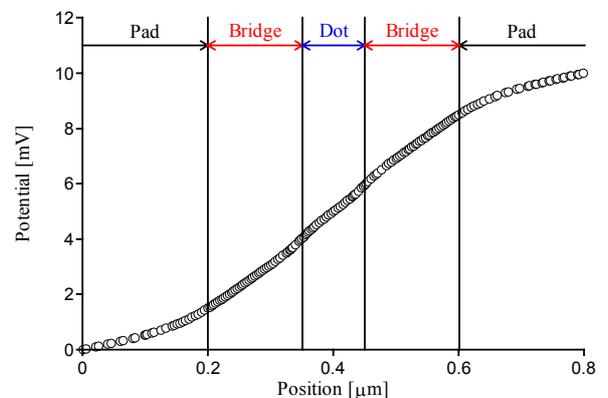


Fig. 4: Potential drop on the solid line in fig.3