Transient response analysis of programming/readout characteristics for NEMS memory

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Introduction

Recent progress of silicon nanofabrication techniques has enabled to explore a new field of silicon Nano Electro-Mechanical Systems (NEMS) research. Since the characteristic frequency of electromechanical systems, in principle, increases in inverse proportion to their sizes, the NEMS have a possibility of extremely high-speed operation [1]. We proposed a new non-volatile memory device concept based on mechanically-bistable operation of the floating gate (FG) in the cavity, combined with nanocrystalline Si (nc-Si) dots as single-charge storage (Fig. 1) [2] and analyzed the mechanical and electrical properties by using the finite element simulation [3, 4]. In this paper, we analyzed the transient responses of the switching and the readout operations of the NEMS memory by using the 2-D finite element simulation combined structural mechanics, electrostatics and drift-diffusion.

Steady-state properties

The structure used for the present simulation is shown in Fig.2. Since 3-D simulations require much computing resources, we conducted the 2-D simulation. A silicon layer is used instead of the nc-Si layer for simplicity. We assumed that the surround of the structure was physically fixed. For realistic modeling of the FG, we introduced the internal compressive stress into the suspended beam. We assumed that negative charges are introduced into the silicon layer. The substrate and source were grounded, and the drain voltage was kept at 0.5 V. The gate voltage V_g was swept.

Under these conditions, we first performed the steady-state analysis to obtain the switching and readout voltages. We calculated the beam displacement and the drain current with changing V_g. As the FG is negatively charged, the upward bent state is the ON state (high current) and the downward bent state is the OFF state (low current). As shown in Fig.3, the memory state switched at V_g = 6 V and -6.7 V. By assuming the readout voltage of 5.5 V, the ON/OFF current ratio was estimated to be about 10^7.

Switching and readout response times

Next we performed the transient analysis to obtain the temporal response times of the NEMS memory for the switching and readout operations. Internal and external damping factors are vital for conducting the temporal response analysis. However, neither theoretical nor experimental estimates of the damping coefficients are available at present for our device structure. In the present work, therefore, we calculated the beam displacements and drain current responses with various values of the damping coefficient β for the OFF state. We applied a 5.5 V step voltage to the gate. As shown in Figs.4 and 5, the transient response times vary from about 90 ns to over 180 ns. The speed of beam motion decreases with increasing β. On the other hand, the beam remains vibrating for a while though the switching motion gets faster with smaller β. We found that β of 2×10^{-10} s was the best among the four values used for the present simulation.

By using β of 2×10^{-10} s as an optimized damping parameter, we calculated the transient response times for the readout and switching operations. Figure 6 shows the transient response with applying a 5.5 V step voltage to the device at the ON state. The current reached the steady state within about 20 ns. Figs.7 and 8 show the switching operations calculated by applying pulse voltages of 7.5 V, 28 ns and -7.5 V, 33 ns, respectively. The applied voltage was chosen larger than the switching voltage obtained from the steady-state analysis since higher voltages achieve faster switching. Apparently we have a tradeoff between the switching time and voltage, and, for the present case, we obtained the switching time of about 80 ns while the gate voltage of 7.5 V.

Summary

We analyzed the switching and readout properties of the NEMS memory. We found that the damping factor influences highly on the transient response time and is important for the fast operations. By assuming the best damping parameter, the transient response times for the readout operation were found about 20 ns and 90 ns for the ON and OFF states, respectively. And the switching time was about 80 ns for the 7.5 V gate voltage.

References

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[3] T. Nagami *et al.*, IEEE Trans. Electron Devices **54**(5), 1132 (2007)

[4] T. Nagami *et al.*, Abstr. Of Si Nanoelectronics Workshop, p.109, 2006

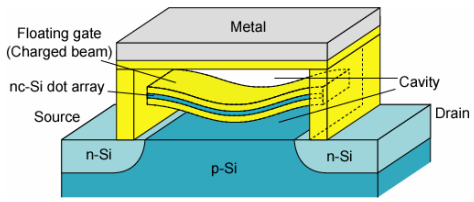

Fig.1: Schematic illustration of a NEMS memory device

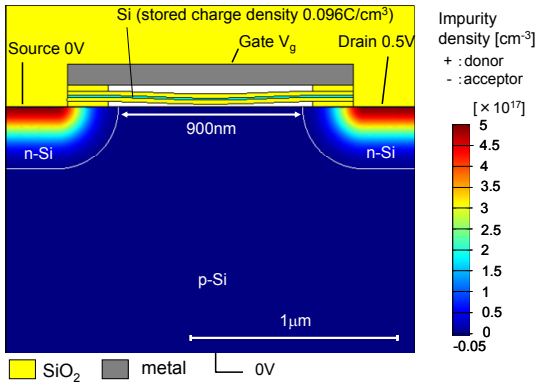

Fig.2: 2-D structure for simulation

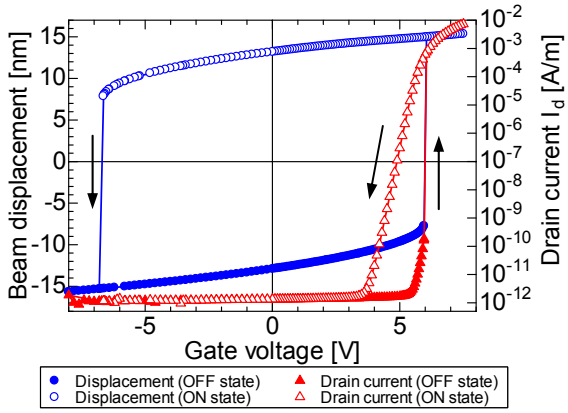

Fig.3: Steady state properties of beam displacement and drain current properties

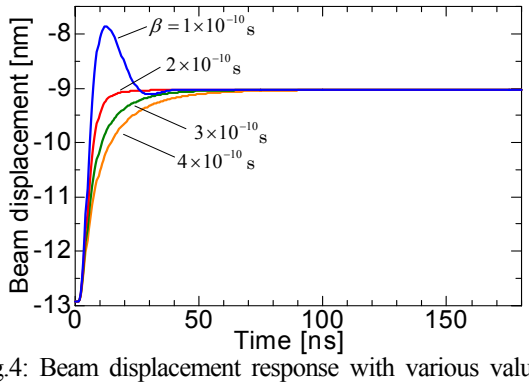

Fig.4: Beam displacement response with various values of damping coefficient β for OFF state. V_g is 5.5 V step voltage.

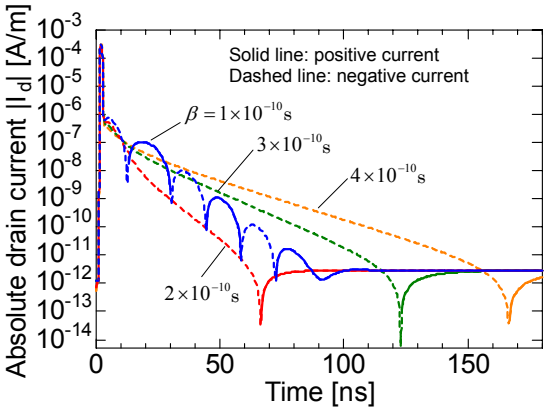

Fig.5: Drain current response with various values of damping coefficient β for OFF state. V_g is 5.5 V step voltage.

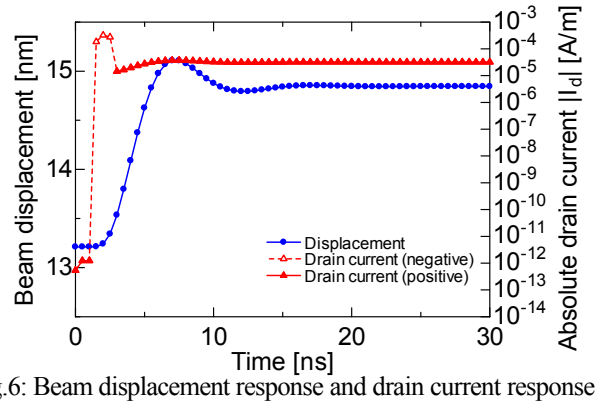

Fig.6: Beam displacement response and drain current response for ON state with applying 5.5 V step voltage to gate.

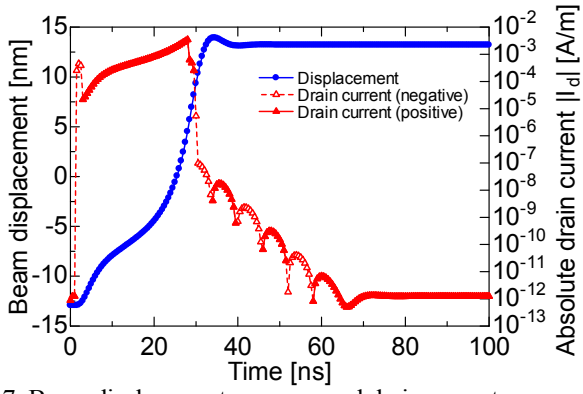

Fig.7: Beam displacement response and drain current response in OFF to ON switching. V_g is 7.5 V, 28 ns pulse voltage.

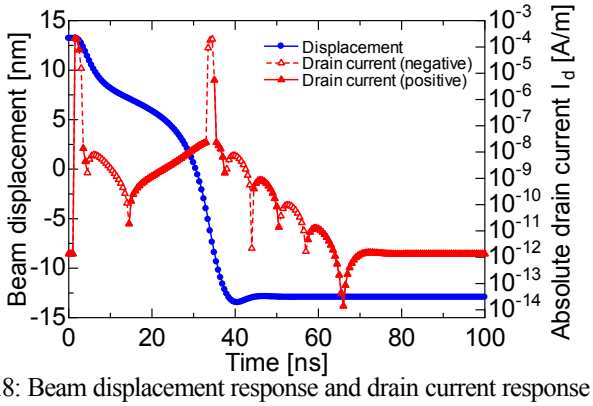

Fig.8: Beam displacement response and drain current response in ON to OFF switching. V_g is -7.5 V, 33 ns pulse voltage.