Is it possible to avoid uncontrolled multiple tunnel junctions induced by random dopants in heavily-doped silicon single-electron transistors?

M. Manoharan[1], Yoshishige Tsuchiya[1, 4], Shunri Oda[1,4], and Hiroshi Mizuta[2, 3, 4]

[1]Quantum Nanoelectronics Research Center, Tokyo Institute of Technology,
2-12-1 O-okayama, Meguro-ku, Tokyo, Japan. e-mail: mano@neo.pe.titech.ac.jp
[2] School of Electronics and Computer Science, University of Southampton, Southampton Hampshire, UK
[3]Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan
[4]SORST JST (Japan Science and Technology Agency)

1. Introduction

Silicon single electron devices (SEDs) have been studied widely for various applications due to their low power consumption and multi-functionality [1]. One of the common approaches to realize single electron devices in silicon is to use very narrow doped silicon channels. In these devices, islands are formed either by the surface roughness and/or random dopants or lateral structural confinement [1, 2]. But, these devices often exhibit multiple tunnel junction (MTJ) behaviours irrelevant to their geometrical shapes [3]. The MTJ characteristics are attributed to the formation of additional tunnel junctions and dots in the narrow channel confinement regions due to potential fluctuation induced by the random dopants or surface roughness. In this paper, we demonstrate that it is possible to overcome the issue of uncontrolled MTJ formation by fabricating extremely short and narrow bottleneck-shaped constrictions with low surface disorder.

2. Fabrication Process

We used an SOI wafer with a 40-nm-thick Si layer (P-doped of ~10^{19} cm^{-3}) and a 200-nm-thick buried-oxide (BOX) layer. Lateral constrictions in the channel were patterned by using the electron beam lithography and subsequent reactive ion etching. After etching, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of SOI. An SEM image of the typical fabricated device structure is shown in Fig.1 (a). The bright and dark regions indicate SOI and BOX layers, respectively. Fabricated lateral constriction length and width are 60 and 30 nm for Device A [Fig. 1(b)] and 25 and 30 nm for Device B [Fig. 1(c)], respectively.

3. Measurement Results and Discussion

Fig. 2 shows the contour plot of the differential conductance as a function of V_d and V_{G3} for Device A. A virtually uniform oscillation period manifests that a single charging island is responsible for the Coulomb oscillation. It should be noticed that there is no periodic lifting blockade. It is attributed to the formation of additional multiple dots in the narrow lateral constriction regions due to the random potential induced by the dopants. Fig. 3 shows the drain current with respect to V_{G3} measured at various temperatures for Device A. It can be seen that the Coulomb oscillation with the oscillation period of ~125 mV (superimposed on the drain current) gradually disappears with the increase in temperature. This indicates that shorter Coulomb oscillation period is due to the island defined by the lateral confinement of the channel. As expected, anomalous oscillation due to the smaller multiple dots induced by dopants disappeared at a higher temperature.

Fig. 4 shows the I_d Vs V_{G1} for Device B at various V_d. The coulomb oscillation with a single oscillation period was observed over a wide gate voltage range. Periodic lifting of Coulomb blockade, for a wide range of V_{G3} voltage in the differential conductance plot for Device B (Fig. 5), indicates the presence of exactly one island in the channel (horizontal white stripes are due to our measuring instrument limitation). This is presumably because that very short constrictions (35 nm shorter than Device A) prevents the formation of the dopant-induced MTJs. The drain current contour plotted as a function of two side gate voltages (V_{G1} and V_{G2}) is shown in Fig. 6 for Device B. Parallel current peak lines with about 59 energy levels are clearly seen, proving that formation of multiple dots is suppressed.

4. Conclusion

The SEDs with relatively long constriction regions invariably exhibit the MTJ characteristics due to the dopant induced potential fluctuation. We clarified that the formation of such uncontrolled MTJs can be avoided by making the constrictions

extremely short and with low surface roughness.

References

[1] Y. Takahashi *et al J. Phys.: Condens. Matter,* **14** R995-R1033 (2002).

[2] R. A. Smith and H. Ahmed, *J. Appl. Phys.* **81**, 2699 (1997).

[3] R. Augke *et al Appl. Phys. Lett.* **76**, 2065 (2000).

Acknowledgement

The authors thank Y. Kawata for the helpful discussions.

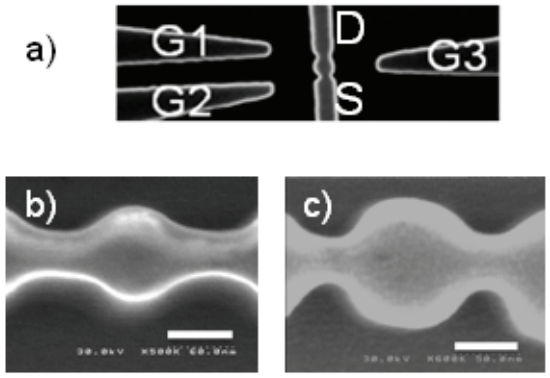

Fig.1. a) SEM image of the fabricated silicon SET, b) Device A dot region (scale bar: 60nm) c) Device B dot region (scale bar: 50nm).

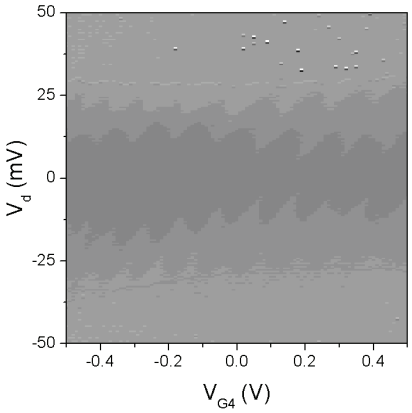

Fig. 2 Differential conductance plot of Device A as a function of V_d and V_{G3} with V_{G1}= V_{G2} = 0V at 4.5K.

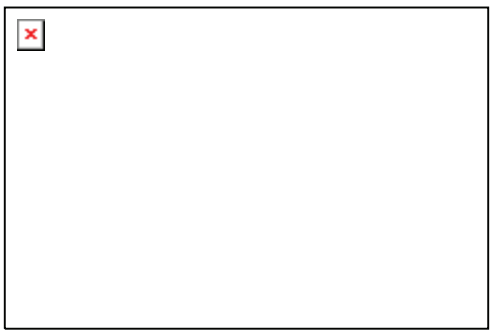

Fig. 3 Drain current plot as function of $V_{G3}$for various temperatures for Device A at V_d = 10mV.

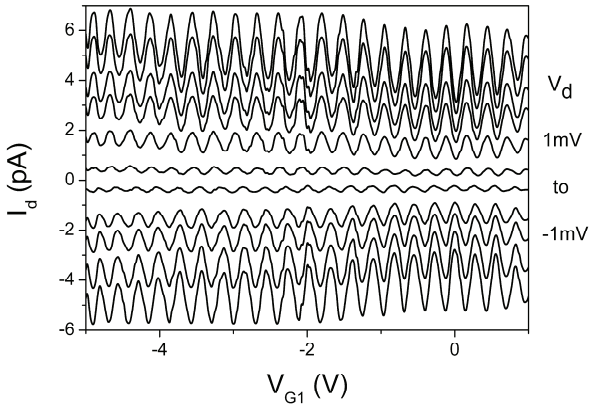

Fig. 4 Drain current as a function of V_{G1} for the drain voltages from 1mV (top) to -1mV (bottom) at 4.2K for Device B.

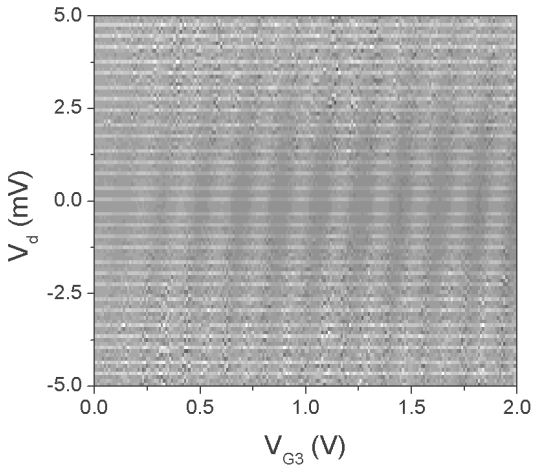

Fig. 5 Differential conductance plot of Device B as a function of V_d and V_{G3} with V_{G1}= V_{G2} = 0V at 4.2K. Horizontal white stripes are due to our measuring instrument limitation.

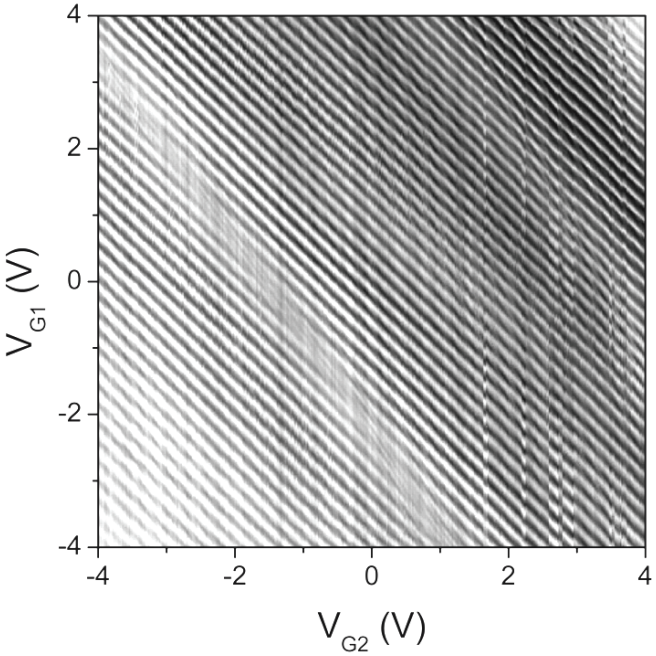

Fig. 6 Contour plot of drain current vs V_{G1} and V_{G2} at 4.2 K of Device B with V_d = 0.1 mV, V_{G3}=0 V.