Observation of Quantum level spectrum for Silicon Double Single-Electron Transistors

Y. Kawata[1,2,5], T. Yamaguchi [2], K. Ishibashi[2], Y. Tsuchiya[1,3,5], S. Oda[1,5], and H. Mizuta[3,4,5]

[1]QNERC, Tokyo Institute of Technology, 2-12-1, O-okayama, Meguro-ku, Tokyo 152-8552, Japan
Phone: +81-5734-3854 FAX: +81-5734-2542 e-mail: kawata@neo.pe.titech.ac.jp
[2]Advanced Device Laboratory, The Institute of Physical and Chemical Reserch (RIKEN), Saitama, Japan
[3]School of Electronics and Computer Science, University of Southampton, Southampton, UK
[4]Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan, [5]SORST-JST

1. Introduction

Double quantum dots (DQDs) have been studied as attractive candidates for charge qubits. Initially, GaAs-based DQDs formed by means of surface gates depletion were studied because many parameters are tunable after their fabrications [1]. However, silicon-based DQDs are more promising for charge qubits because of the absence of piezoelectric electron-phonon coupling, and the effect of phonon localization [2]. Furthermore, to integrate Si multiple charge qubits and a readout device in a small footprint, a series-connected double dots transistor has recently been proposed and studied [3]. The readout is called as double single-electron transistors (DSETs) and facilitates to detect the single-charge polarizations on the adjacent double qubits efficiently [4]. The other advantage of DSETs is that both two SETs act as feedback transistors to each other to compensate the random fluctuation noise.

It is also important to clarify the quantum effects in the vicinity of the charge triple points from a standpoint of future down-scaling of the DSETs and qubits. However, the impacts of quantization on single-electron tunneling characteristics have not been studied for lithographically-defined silicon DQDs. In this paper, we report on the tunnel spectroscopy of quantum levels on lithographically-defined silicon DSETs at milli Kelvin temperatures for the first time.

2. Fabrication of DSETs

The DSETs were fabricated on the SOI substrate with the SOI thickness of 40 nm and the phosphorous doping concentration of 10^{19} cm^{-3}. An SEM image of the fabricated DSETs with control gates (G3-G7) for qubits (to be integrated) and the equivalent circuit of DSETs are shown in Fig. 1(a) and Fig. 1(b), respectively. After lithography and etching to pattern the DSETs, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the thickness of the SOI down to 30 nm. This results in an overall core dot diameter of approximately 55 nm. In this device structure, the adjacent constrictions act as tunnel barriers connecting the dots to the source and drain electrodes.

3. Electrical characteristics for DSETs

Electrical measurements were carried out at the dilution base temperature of 22 mK and the effective electron temperature of around 0.2 K. Figs. 2 (a) and 2 (b) show the contour plot of I_D measured and simulated respectively as a function of V_{G1} and V_{G2} at V_{DSeff}=-7.5 mV, where V_{DSeff} is the voltage drop between the leftmost and the rightmost barriers. The simulation reproduces the measured characteristic because the dots are well defined. From this measurement characteristic, the total capacitances of Dot 1 and Dot 2 and the inter-dot capacitance were extracted to be C_{C1}=16 aF and C_{C2}=12 aF, and C_{Cm} =3.1 aF, respectively. The corresponding charging energies are E_{C1}=10 meV, E_{C2}=14 meV, and E_{Cm}=2.7 meV. Additionally, gate capacitances C_{G1D1}=0.75 aF, C_{G1D2}=0.50 aF, C_{G2D2}=0.80 aF, and C_{G2D1}=0.70 aF were also extracted from the characteristics. Similar stability characteristics were observed at 4.2 K, and the extracted gate capacitances of the dots were almost the same as those extracted at dilution temperature of 22 mK. With this consistency in the device characteristics at different temperatures, the origin of the dots is attributed to the well-defined lateral confinements.

A fine sweep across the charge triple points is shown in Fig. 3 (a). In this measurement, a primary sweep was done with the gate G1. This gray scale plot displays the values of differential conductance ($\partial I_{DS}/\partial V_{G1}$) as a function of V_{G1} and V_{G2} for V_{DSeff}= -8.5 mV. Fig. 3 (b) blows up the square region marked in Fig. 3 (a) and I_D-V_{G1} characteristics along the dotted line in the ($\partial I_{DS}/\partial V_{G1}$) plot. The current peaks in I_D-V_{G1} plot are located between differential conductance peaks in the triangle-shaped region in ($\partial I_D/\partial V_{G1}$) plot. These current peaks and ($\partial I_D/\partial V_{G1}$) peaks are caused by the resonant tunneling through DQDs. These high ($\partial I_D/\partial V_{G1}$) peaks can be used to detect single-charge polarizations for double qubits integrated in the future. Given that all the level intervals are the same for two dots, the energy spacing was estimated to be 0.5 meV. This value is in good agreement with the value of 0.6 meV estimated from the dot diameter of 55 nm. Inelastic tunneling rate between the dots Γ_i is also estimated to be 3.0×10^6 Hz at most from the off-resonance current $I_{off}\approx$ 0.48 pA at V_{G1}=0.835 V along the dotted line in Fig. 3 (b). Because of the present device geometry (Fig. 1(a)), the inter-dot tunneling rate at resonance Γ_{LR} is considered to be smaller than Γ_L and Γ_R, and is dominant where $\Gamma_{LR}\approx3.6\times10^6$ Hz can be estimated from the resonant current 0.58 pA at V_{G1}=0.843 V along the dotted line in Fig. 3 (b). Finally, the peak-to-valley current ratio is evaluated to be 1.2.

3. Conclusions

We observed the spectrum of quantum levels for silicon DSETs, which is composed of DQDs. The quantum dots were attributed to the well-defined lat-

eral confinement even at the dilution base temperature of 22 mK. The estimated level spacing in quantum dots from the characteristics was also in agreement with the value from the quantum dot size. The inelastic tunneling rate between dots was quite small compared with GaAs-based DQDs. The observed differential conductance peaks can be used to detect double qubit integrated in the future.

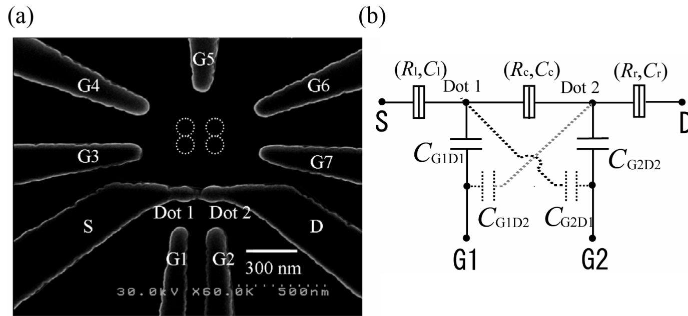

Fig. 1 (a) SEM image of DSETs and qubits gates (G3-G7). The dotted circles indicate the DQDs integrated in the future. (b) The equivalent circuit of DSETs.

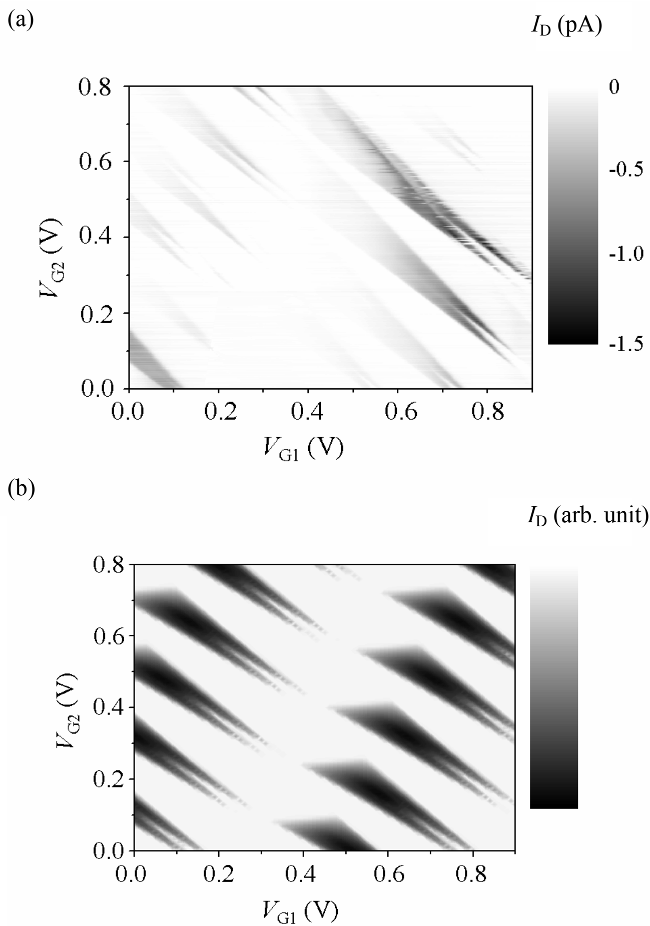

Fig. 2 Contour plot of I_D (a) measured and (b) simulated as a function of V_{G1} and V_{G2} at V_{DSeff} =-7.5 mV at dilution base temperature of 22 mK.

References

[1] T. Fujisawa *et al.*, Physica E **21**, 1046 (2004).

[2] J. Gorman *et al.*, Phys. Rev. Lett., **95,** 090502 (2005).

[3] Y. Kawata *et al.*, SNW 2007, pp.119 (2007).

[4] Y. Kawata *et al.*, SSDM 2007, pp.1126 (2007).

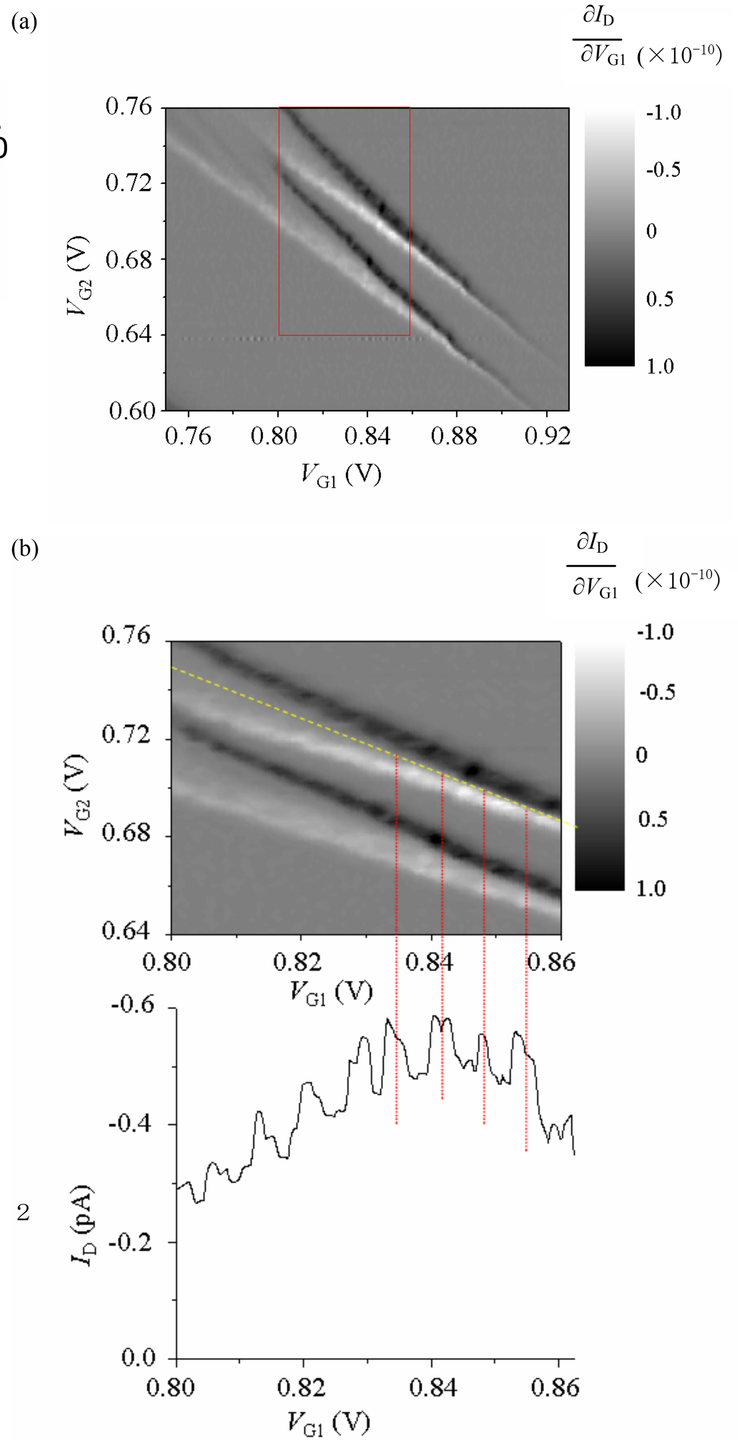

Fig.3 (a) Contour plot of differential conductance ($\partial I_{DS}/\partial V_{G1}$) as a function of V_{G1} and V_{G2} at V_{DSeff}= -8.5 mV. (b) The square region marked in Fig. 3 (a) and I_D-V_{G1} characteristics along the dotted line in the ($\partial I_{DS}/\partial V_{G1}$) plot are shown.