Controlled Ge Nanowires Growth on Patterned Au Catalyst Substrate

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1.Introduction

One-dimensional semiconductor nanostructures have attracted much attention because of their potential applications in the design of novel electronic, photonic, and sensing devices. Due to their high mobility of electrons and holes, Ge nanowires are particularly attractive for high-speed field-effect transistors. Moreover, Ge nanowires are potentially useful for building quantum bits because of a long decoherence time due to a predominance of spin-zero nuclei [1] and the advantage of a large excitonic Bohr radius (24.3 nm) which allows the quantum confinement to be observed for relatively large structures [2] and at high temperatures. To realize these applications on a large scale, one of the key challenges is to develop a convenient and parallel method to align bottom-up nanowires into complex patterns or structures [3]. Recently, a "pick and place" method is most widely used for integrating nanowires. However, these processes lack control in precision, repeatability, and easily induce contamination and defects in the wires [4]. It is expected to selectively grow nanowires directly onto desired areas of the substrate and *in situ* fabricate the nanowire devices [5]. In the VLS (vapor-liquid-solid) CVD process, gold catalysts initiate and guide the growth of nanowires. Hence, precise control the location of nanowires relies on the capability to control the location of Au clusters. In this paper, we demonstrate the well location-controllable Ge nanowires on SiO_2 substrate by combining top-down and bottom-up methods.

2.Experimental details

The Ge nanowires were grown by using a low pressure CVD method with 10% GeH_4 precursors (in an atmosphere of hydrogen) in a total pressure of 5 Torr at 300 ^oC on the patterned Au catalyst on SiO_2. All the Au particles were evaporated by electron beam evaporation at room temperature with a thickness of 0.5 nm. Well-ordered Au catalysts were prepared by using a JEOL JBX-5DII electron-beam lithography (EBL) system with a beam voltage of 50 kV and a beam diameter of 8 nm and a lift-off method. Fig.1 shows the schematic of the process for patterning Au catalysts and growth of Ge nanowires.

3.Results and discussion

Fig.2 shows the SEM images of high-density Ge nanowire strips with the width of 10 μm and 200 nm, respectively. Ge nanowires with diameter of 5 ~ 20 nm can be grown selectively on the area with Au catalysts. High-resolution TEM images reveal the high-quality single-crystalline Ge nanowires with a lattice constant of 0.565 nm, which is in excellent agreement with the diamond crystal structure known for Ge. By reducing the size of the Au pattern to contain only a few Au particles, the Ge nanowire array with the space distance of 10 μm was obtained (Fig.4). There are several wires (about 10) in each area as shown in the inset to Fig.4. In order to realize the alignment of single Ge nanowire, the Au catalyst array with only one Au dot in each area is needed. By optimizing the EBL process and controlling Au density by adjusting the deposition speed and thickness of Au, well-ordered single Au dot array with a space of 700 nm was prepared as shown in Fig.5. Each Au dot has a diameter of around 10 nm (Fig.5B). On such Au catalyst array, we succeeded to grow the array of a single Ge nanowire with a space of 700 nm. The SEM image in Fig.6 shows that only one wire was grown on each Au pattern and the Ge nanowires are located precisely where the Au catalysts sit.

4.Conclusion

A well-ordered array of single Ge nanowires was grown by LPCVD method on the patterned Au catalyst substrate. Ge nanowires can be grown selectively on the area with Au catalysts. By controlling the location of Au catalysts, we can precisely control the growth of Ge nanowires, which may offer the possibility of *in situ* fabrication of nanowire devices.

References

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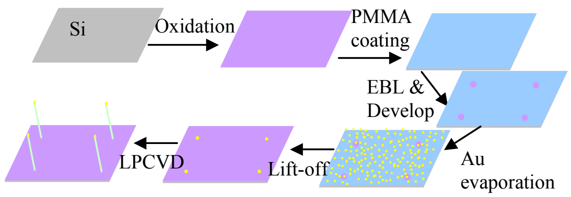

Fig.1 The schematic of process for patterning Au catalysts and growth of Ge nanowire

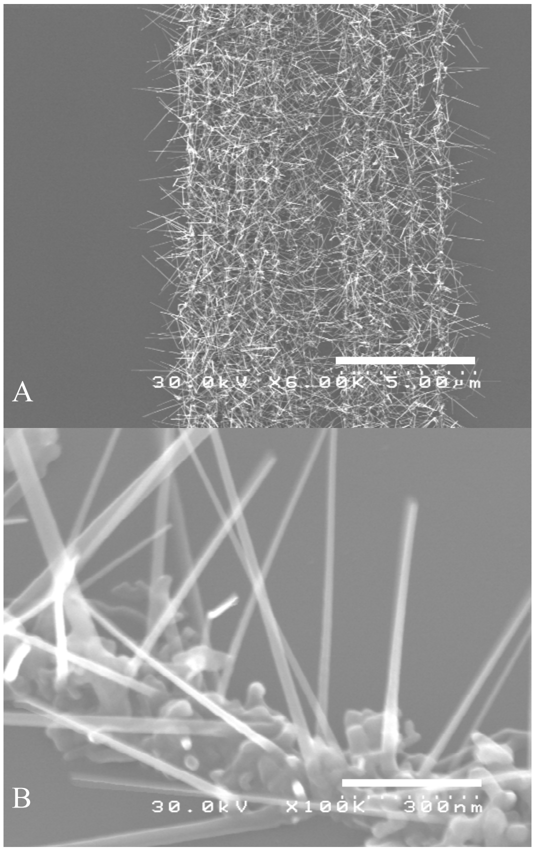

Fig.2 SEM images of Ge nanowires strips with the width of 10 μm(A) and 200nm(B) grown on SiO_2 substrate

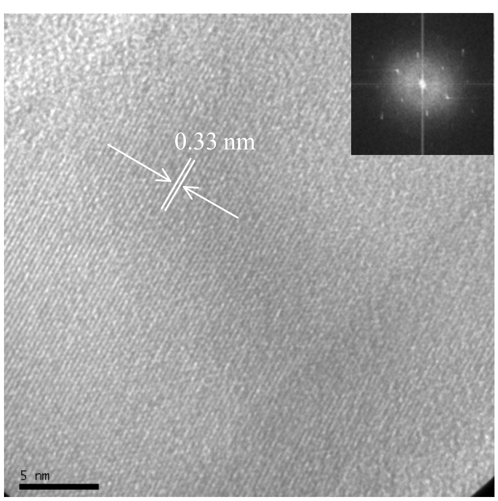

Fig.3 High resolution TEM image of Ge nanowires and its fast Fourier transform image(inset).

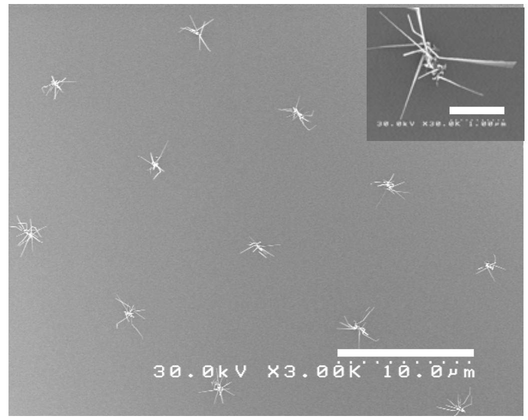

Fig.4 SEM images of Ge nanowires array with the space distance of 10 μm. The inset is the enlarged image of one pattern. The scale bar in the inset is 1 μm.

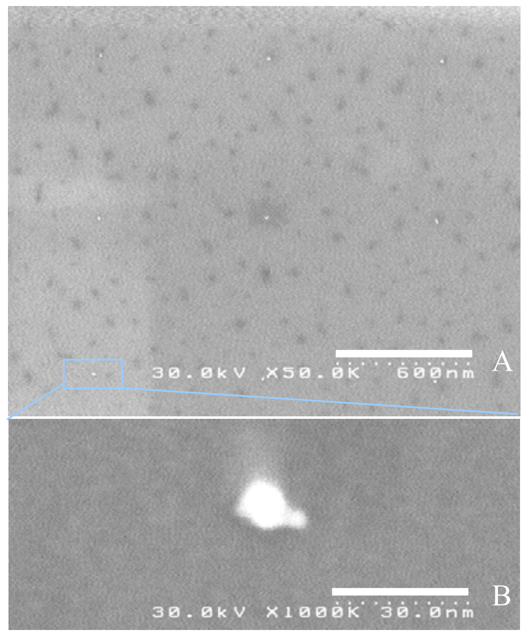

Fig.5 SEM images of patterned Au dots with space of 600nm(A); The enlarged image of one Au dot with the diameter of 10 nm(B)

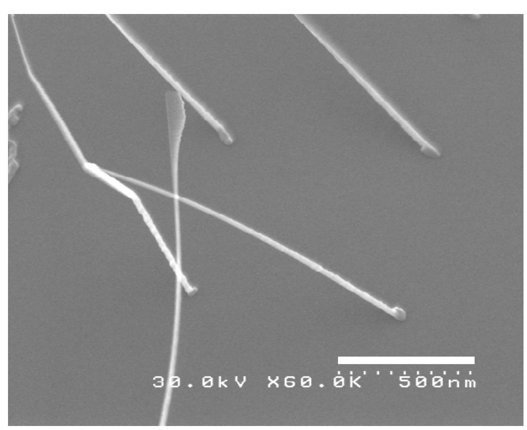

Fig.6 SEM images of single Ge nanowire array grown on Au catalyst pattern.