

Design Optimization of NEMS Switches for Single-Electron Logic Applications

Benjamin Pruvost¹, Hiroshi Mizuta^{2,3}, and Shunri Oda^{1,3}

¹QNERC, Tokyo Institute of Technology 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, JAPAN

²School of Electronics and Computer Science, University of Southampton, SO17 1BJ, United Kingdom

and ³SORST JST (Japan Science and Technology)

E-mail: benjamin@neo.pe.titech.ac.jp, Phone: +81-3-5734-2542, Fax: +81-3-5734-2542

1. Introduction

Hybrid devices coupling single-electron transistors (SETs) to nano electromechanical systems (NEMS) have recently drawn much attention for their promised experimental insight into quantum aspects of mechanical systems as much as for their potential applications in communication and information technology. Some groups exploited the ultra high sensitivity of the SET to read out the motion of a capacitively coupled nanomechanical resonator, managing to approach its quantum limit [1], [2]. Another group proposed an SET whose island is located at the top of a free-standing silicon nanopillar shuttling between the source and the drain [3]. Finally, a suspended-gate architecture, which would enable to switch the SET gate capacitance between two values, has been suggested in [4, 5], although no study on its actual performances has yet been conducted.

In this work, we focus on the design optimization and the analysis of the latter device in order to evaluate its merit and demerit. We propose a realistic low-voltage window design methodology, which could actually also be used for systematical design of conventional NEMS switches. We also demonstrate some applications that arise from the movable gate, such as a way to cope with the random background charge problem and to build logic functions.

2. Design Optimization and Performance Analysis

The principle of the suspended-gate SET is depicted in Fig. 1: it combines a conventional SET and a tunable NEMS capacitor which acts as a two-state capacitive switch with a pull-in voltage V_{PI} . Although simulation basically authorizes any dimensions for the cantilever, some theoretical constraints have to be imperatively respected for the structure to be viable. In particular and in contrast to micromechanical switches, the Casimir force cannot be neglected at the nano-scale and imposes a maximal length to the beam not to stick to the substrate, called the detachment length [6]. Taking account of this constraint, we solved the 3-D coupled electromechanical equation for conventional cantilevers. Fig. 2 shows the calculated low-voltage actuation ($<1V$) design windows for different aluminum cantilever thicknesses. We then optimized the cantilever shape in order to minimize the actuation electrode area, and we simulated the optimized structure both statically (Fig. 3) and dynamically (Fig. 4) by using the 3-D simulator COMSOL [7]. The proposed design offers low-voltage actuation ($\sim 1V$) and fast switching ($<50ns$). Fig. 5 also shows that the thickness of the oxide covering the actuation electrode can efficiently be chosen to adjust the value of the movable gate capacitance in the ON state.

The total energy consumed in the switching process consists of two main parts, namely the electrical energy stored in the NEMS capacitor and the mechanical energy

stored in the cantilever spring, and is given by $E = E_e + E_m = \frac{1}{2} C_{gap} V^2 + \frac{1}{2} k t_{gap0}^2 \approx 0.02fJ$ for the dimensions under consideration. For comparison, the minimum switching energy achieved by the present CMOS technology is 0.1 fJ.

3. Single-Electron Logic Application

Random fluctuations of static and dynamic background charge, which can alter the operating characteristics of the device, are a serious problem faced by the SET. Rather than trying to suppress these effects, one solution is to make the information insensitive to them by getting the necessary redundancy from the amplitude or the periodicity of the oscillations [8]. The periodicity of the Coulomb oscillation governing the SET characteristics being given by e/C_G , and its amplitude by e/C_Σ (where C_G is the capacitance between the gate and the island, and C_Σ the total island capacitance), one can define two distinct states for the device, depending on the gate position, and build logic building blocks (Fig. 6). Because one has to sweep the input voltage over several periods to determine the logic state, such encoding may be considered as slow if compared to direct level encoding. However, the fundamental speed limit of SETs being linked to the speed of quantum mechanical tunneling ($<1ps$), the limiting factor is by far the switching speed of the gate ($\sim ns$), which limits the operation frequency to the GHz range. The low SET voltage gain may be improved by the use of a MOSFET configured to amplify the drain current [5].

4. Summary

We modeled and optimized a NEMS switch cantilever in the aim of modulating the Coulomb oscillation of a conventional SET. Both its static and dynamic characteristics were simulated, and we showed how it is possible to get rid of the unwanted background charge effect for single-electron application. Although the operation frequency is limited to the GHz range due to the switching speed of the cantilever, gain in terms of power consumption and scaling makes it very competitive.

References

- [1] R. G. Knobel *et al.*, *Nature*, Vol. 424, pp.291-293, 2003.
- [2] M. D. LaHaye *et al.*, *Science*, Vol. 304, pp.74-77, 2004.
- [3] D. V. Scheible *et al.*, *Phys. Rev. Lett.*, Vol. 84, No 23, pp. 4632-4634, 2004.
- [4] C. Wasshuber, *Proc. of Design Autom. Conf. 2003*, pp. 274-275.
- [5] S. Mahapatra *et al.*, *Proc of IEDM 2003*, pp. 703-706.
- [6] W.H. Lin *et al.*, *Microsyst. Technol.*, Vol. 11, pp. 80-85, 2005.
- [7] COMSOL, User's guide; see also www.comsol.com.
- [8] Klunder R. *et al.*, *Proc. of ECCTD 2001*, pp. 213-216.
- [9] SmartSpice, User's guide; see also www.silvaco.com.
- [10] B. Pruvost *et al.*, *J. Appl. Phys.*, Vol. 103, pp., 2008.

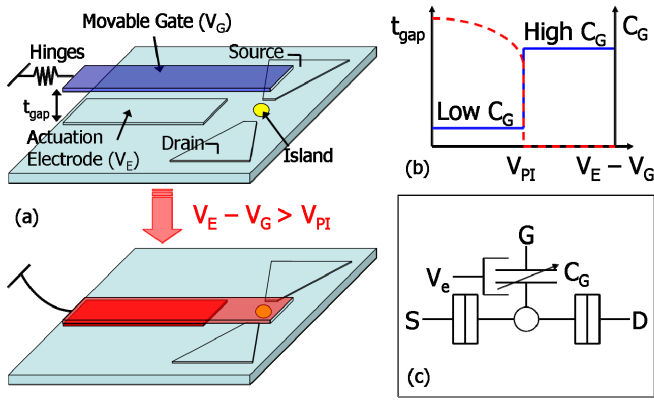


Fig. 1 (a) Concept of NEMS-gate SET device; (b) Gate displacement (left axis) and corresponding capacitance (right axis) vs. actuation voltage; (c) Electrical equivalent schematic.

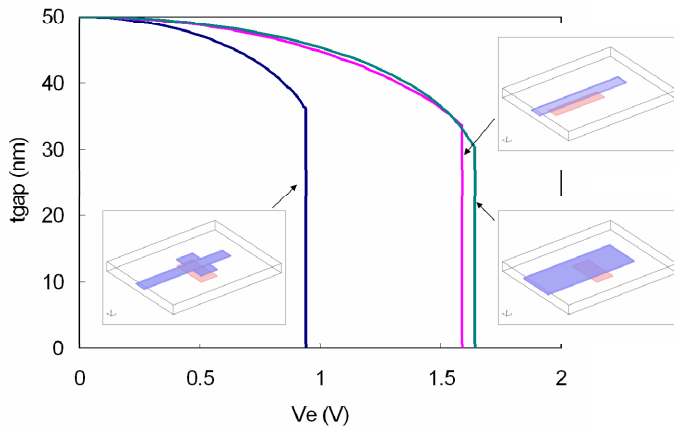


Fig. 3 Static actuation of the optimized cantilever (cross shape, $L=800\text{nm}$, $w=100\text{nm}$, $W=300\text{nm}$, $th=10\text{nm}$) with a 50nm initial air-gap. For comparison, the actuation of two conventional cantilevers with the same overlapping electrode area is also shown.

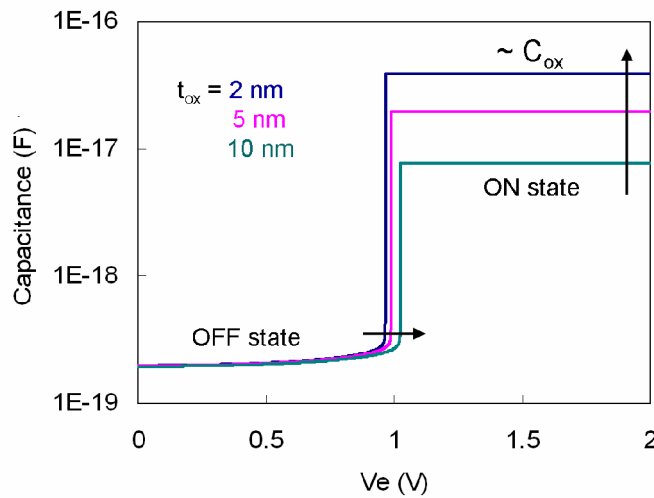


Fig. 5 Estimation of the movable gate capacitance for several oxide thicknesses. Since the thickness does not have a critical influence on the pull-in voltage, it can be efficiently chosen to adjust the gate capacitance in ON state.

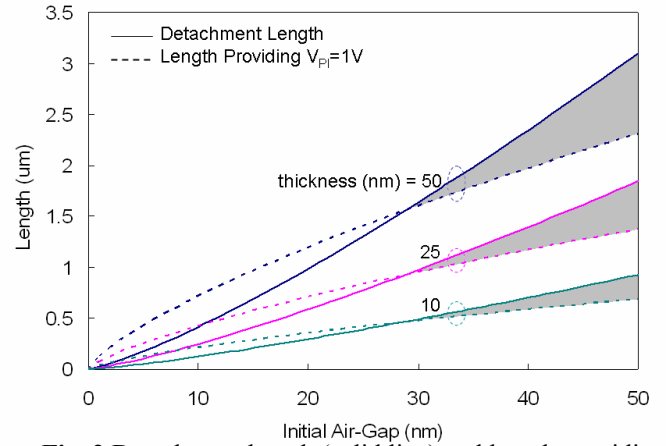


Fig. 2 Detachment length (solid line) and length providing 1V pull-in voltage (dotted line) as a function of the initial air-gap for aluminum cantilevers with various thicknesses. The areas in grey show the $<1\text{V}$ actuation voltage windows. Other areas represent either not viable or $>1\text{V}$ actuation voltage switches.

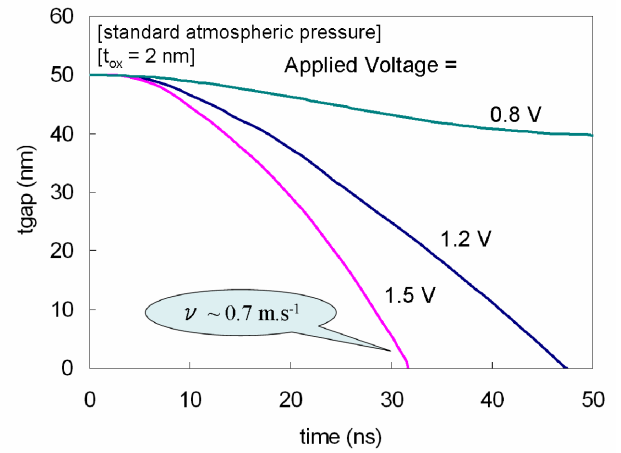


Fig. 4 Dynamic actuation of the optimized cantilever under 1atm . For applied voltages lower than 1V , the beam moves toward its equilibrium position, whereas for applied voltages greater than 1V , it hits the bottom electrode with a pulling time shorter than 50 ns , and the speed of the tip is then less than 1m.s^{-1} .

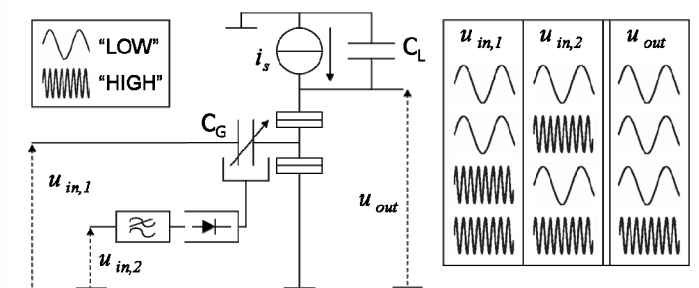


Fig. 6 An implementation of the AND function based on the theory developed in [8]. The period of the signal $u_{in,2}$ determines the voltage applied to the actuation electrode of the NEMS switch and therefore the value of C_G .