Single Electron Transport Simulations in Silicon Nanochains

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Abstract: We carry out simulations of Coulomb staircases observed experimentally in the current-voltage (*I-V*) characteristics of single Si nanochains at room temperature [1]. The nanochains consist of Si nanocrystals (SiNCs) ~10 nm in diameter, separated by ~5 nm SiO_2 barriers. Coulomb staircases characteristics can be simulated using a multiple tunnel junction (MTJ) model (Figure 1 (a)) [2]. Here, the SiNCs form charging islands, isolated by tunnel barriers at the SiO_2 regions (Figure 1 (b)). Figure 1 (c) shows SEM image of a nanochian. Figure 1 (d) shows the *I-V* characteristics of a nanochain containing 7 SiNCs, similar to experimentally measured devices. We simulate these characteristics using an MTJ with equal junction capacitances (*C*), varying values of junction resistances (R_1, R_2,….,R_n), and equal SiNC to substrate capacitances C_0. Simulations show that the C_0 plays an important role in reduction of the threshold voltage, as shown in Figure 1 (e). As C_0 increases, a greater proportion of the source-drain voltage (V_{DS}) across the nanochain drops across the first tunnel junction, due to the voltage divider formed by the first junction capacitance *C*, and the first stray capacitance C_0, in parallel with the equivalent capacitance of the rest of the MTJ [3]. The charging energy of the first junction is overcome at lower voltages, leading to a lower onset of current. The simulations demonstrate that a random variation in the tunnel junction resistances leads to clearer Coulomb staircases. A 60% variation in resistances gave the best fit to our experimental results.

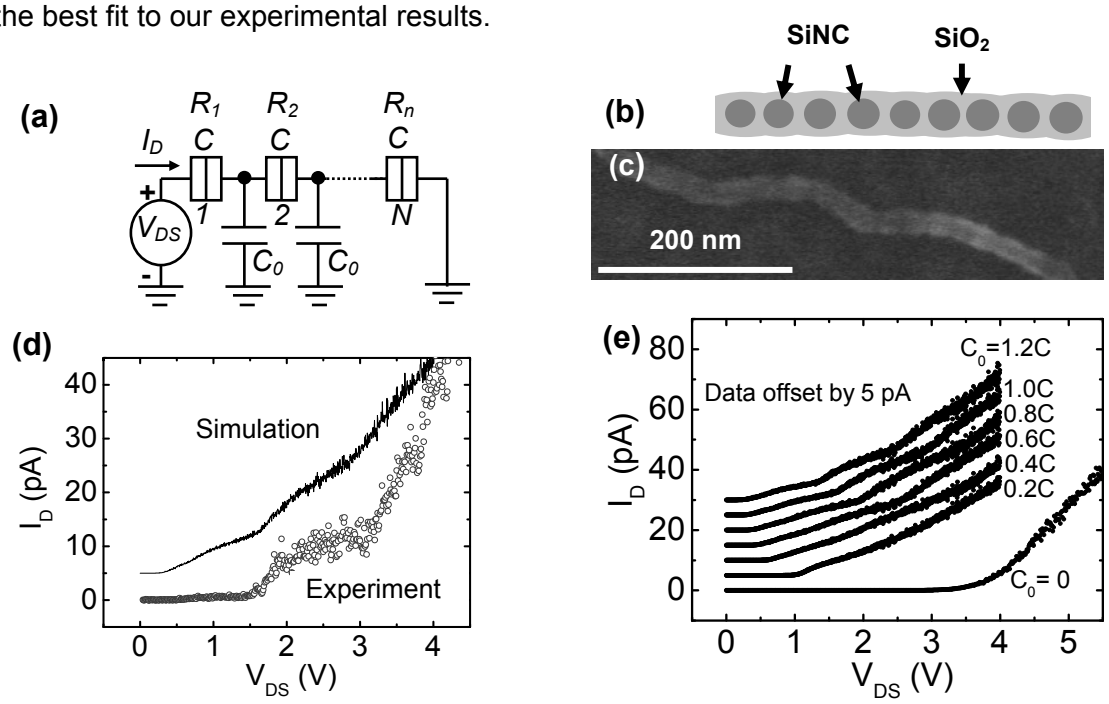

Fig 1: (a) Equivalent circuit diagram of a nanochain device (b) Schematic diagram of a nanochain (c) SEM image of a nanochain (d) Experimental and simulated *IV* characteristics of a nanochain device (e) Simulated effect of gate capacitance on threshold voltage.

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