Hybrid silicon nanotechnologies for advanced information processing

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Abstract: In this paper we present our recent attempts at developing the advanced information processing devices in 'More than Moore' and 'Beyond CMOS' domains. For the 'More than Moore' domain, we introduce our nanoelectromechanical (NEM) memory as an examples of co-integration of the heterogeneous nanotechnology and the conventional CMOS technologies. For the 'Beyond CMOS' domain, we discuss the recent progress of silicon-based quantum information processing (QIP) technologies in terms of hybrid nanofabrication technologies for integrating single and multiple charge qubits with a single-charge detector.

1. Introduction

The dawn of the silicon nanoelectronics was seen when the physical gate length of high-performance of CMOS got shorter than 100 nm in 1999 after continuous down-scaling over the last few decades under Moore's Law. The latest *International Technology Roadmap for Semiconductors* [1] predicts that such top-down approach will be pursued further in the nanoelectronics regime - known as 'More Moore' approach - and the CMOS gate length will reach 9 nm in 2016. However, maintaining such aggressive top-down trend is getting increasingly difficult both technologically and economically because a number of new "technology boosters" should be introduced for the next few years. Under these circumstances present nanoelectronics research is characterized by the migration of research from pure down-scaling to the quest for new functionalities beyond CMOS and hybridization of CMOS and other heterogeneous technologies. Nanoelectronics research may therefore be divided into three main research domains: 'More Moore', 'More than Moore' and 'Beyond CMOS' as shown in Fig. 1. 'Beyond CMOS' domain covers novel device principles which are not based on the CMOS operation and circuit architecture, which may include, spin-based memory and logic devices, quantum information processing (QIP), and other advanced infromation processing devices by using inorganic/organic 'bottom-up' materials such as carbon nanotubes and organic molecules. On the other hand, the 'More than Moore' domain deals with hybrid co-integration of conventional Si CMOS technology and various other technologies such as micro- and nano-electromechanical systems (MEMS/NEMS), nanophotonic devices, sensor devices and RF devices in order to meet certain needs and specifications of advanced system applications. Massive efforts are therefore made now on studying

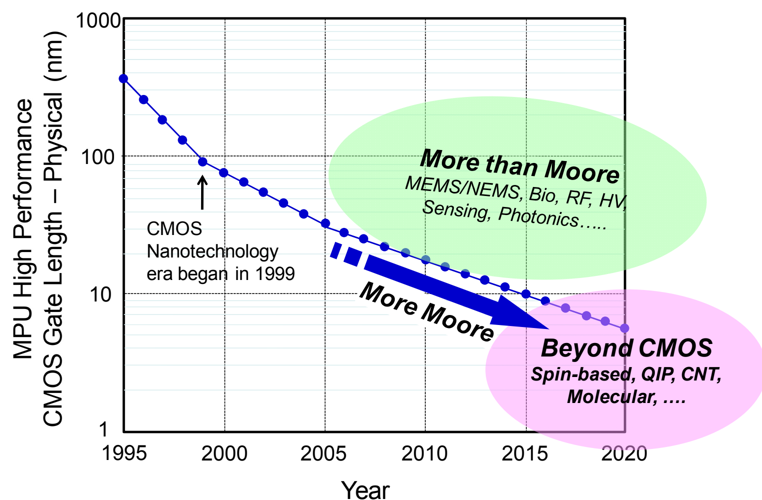

FIG. 1 Three technology domains in silicon nanoelectronics era.

emerging research materials and devices for exploring the new 'More than Moore' and 'Beyond CMOS' domains. In this paper we present our recent attempts to introduce novel silicon nanotechnologies for developing advanced information devices in these two new nanoelecrtonics domains.

2. For 'More than Moore' domain – Co-integration of nanoelectromechanical (NEM) devices and conventional silicon devices

For exploring the 'More than Moore' domain, we chose the NEMS technology among various heterogeneous technologies for the following reason. It is widerly known that microfabrication technilogies matured with the silicon VLSI development in the past decades have opened another vast technology area of MEMS/NEMS. The MEMS have already entered an area of mass production for such as mobile phones and automobiles. It is expected that the MEMS market will grow with the rate of 30 – 40 % per annum and will reach ten billion dollers in 2015. Along with such rapid expansion in MEMS business, there has also been continuous efforts at making the MEMS smaller for raising their operation frequency. For example, the oscillation frequency of over 1 GHz has recently been demonstrated for the 1.1-µm-long SiC based beam [2]. The characteristic length (such as the resonator length) of the semiconductor-based MEMS structures reported for the past decade are plotted in Fig. 2: the MEMS technology has entered the sub-µm regime and is now proceeding towards the nanoscale regime. If we adopt the same definition of 'Nano Era' as that for CMOS, the present trend indicates that the NEMS era would come between 2010 and 2015.

The appearance of high-speed NEMS was tempting enough for us to consider co-integration of the NEMS components into the conventional silicon electron devices for giving extended performance and exploring novel functionalities. As the first attempt, we proposed a new nonvolatile NEM memory in which a mechanically bistable floating gate (FG) is integrated onto the conventional MOSFET (Fig. 3(a)) [3][4]. The FG consists of SiO_2 matrix with the array of the nanocrystalline (nc-) Si dots as single-electron storage and has two structurally-stable states – upward- or downward-bent states. The FG may be flip-flopped via the gate electric field, and its structural states are sensed via a change in the drain current of the MOSFET underneath. Owing to its operating principle, the NEMS memory possesses various tangible advantages over the conventional Flash memory. For example, it is seriously non-volatile as programming / erase operation does not use charge tunneling via the gate oxide, and no gate oxide degradation is therefore anticipated. Programming /erase time can be much shorter than Flash memory by making the beam dimensions into the submicron regime.

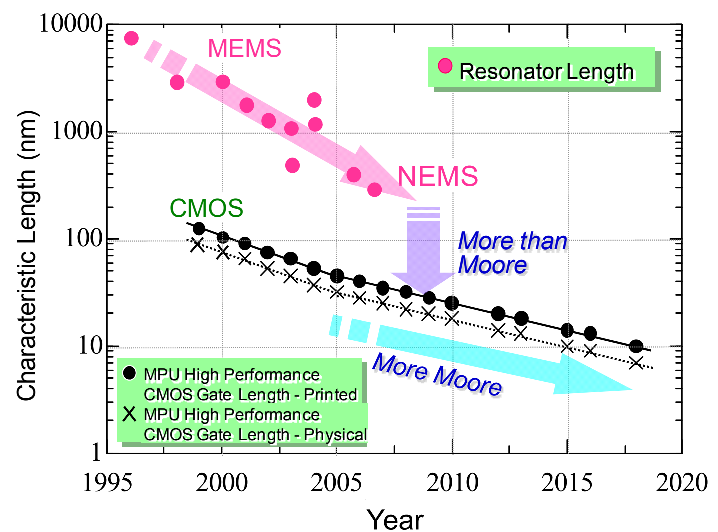

FIG. 2 MEMS down-scaling for the past decade superposed on the CMOS miniaturization trend.

A prototype device structure was fabricated by developing the following process: A 50-nm-thick SiO_2 layer was first formed by oxidizing the surface of a 200-nm-thick SOI. Second, the nc-Si dots of approximately 10 nm in diameter were deposited using the VHF plasma CVD [5] with the areal density of about 5 x 10^{11} cm^{-2}. A 50-nm-thick SiO_2 layer was then deposited by using CVD to sandwich the SiNDs between the double SiO_2 layers. After that a 150-nm-thick amorphous Si layer, a 50-nm-thick SiO_2 layer and a 100-nm-thick Cr layer were deposited sequentially. The control gate was patterned using EB lithography, and the top SiO_2 layer was etched anisotropically. The underneath Si sacrifice layer was then etched out using isotropic dry etching. By repeating this, the upper and lower cavities were formed. Figure 3(b) shows the fabricated FG with the embedded nc-Si dot layer. All the fabricated FGs were bent upward by approximately 50 nm. The FGs were buckled as the stress at the SOI / thermal SiO_2 interface was released by removing the sacrificial Si layer. Degree of bending may be altered by changing the ratio of the stress-free CVD-grown SiO_2 thickness to the thermal SiO_2 thickness.

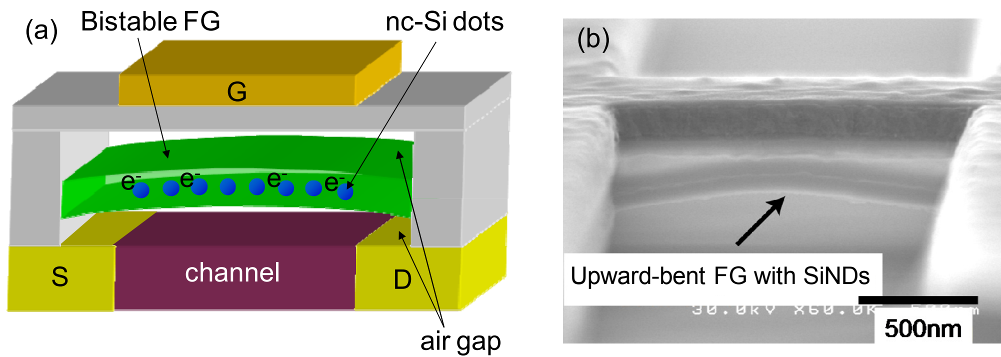

FIG.3 (a) Concept of high-speed and nonvolatile memory and (b) a prototype device structure

The electrical readout characteristics were studied by performing 3D hybrid simulation of mechanical, electrostatic and electron transport equations. One of the key issues for designing the NEMS memory is to meet two requirements of redcing the switching voltage and maintaining the current ON/OFF ratio large enough for readout simultaneously. Overall optimization is therefore needed for the structural and material parameters of not only the FG but also outer cavity. Figure 4 shows I_d-V_g characteristics calculated for the bistable states of the FG with various values of the zero-bias bending Z_0. The results indicate that our NEMS memory may exhibit the ON/OFF ratio as high as 10^5 and the threshold voltage shift ΔV_t of over 2 V. The associated switching voltage is made less than 10 V.

The switching speed of our NEMS memory was also studied by performing transient analysis by taking account of damping phenomena after the FG switched to its ON/OFF states. The simulated results showed that the switching time shorter than 50 nsec is achieved for the NEMS memory with a 1-µm-long FG while it can further be decreased by optimizing the applied gate voltage. Apparently further switching voltage reduction is needed

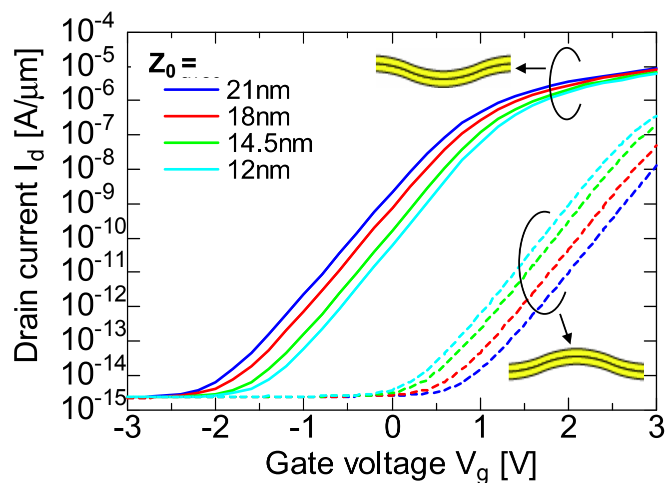

FIG. 4 I_d-V_g characteristics for the bistable FG states with various different initial bending Z_0.

in order for competing with other candidates of emerging nonvolatile RAMs such as MRAM, FRAM and PCRAM. However, it is certainly an advantage for the NEMS memory in contrast with the other candidates that it can be manufactured within the conventional Si technologies without introducing any exotic materials.

3. For 'Beyond CMOS' domain – Progress towards Si-based quantum information processing

Among a variety of emerging nanotechnologies explored in the 'Beyond CMOS' domain, QIP is a particularly challenging one as it relies on coherent nature of electrons (or their spins) in silicon which we have not tackled in the conventional technologies. The elementary units for realizing QIP systems are quantum bits (qubits) – two-level quantum systems. In principle, we have a number of potential candidates as a physical implementation of a qubit, either a native or artificial entity, for example, charge states or spin states in quantum dots, superconducting charge states or flux states, nuclear spins, photons, excitons, and so forth. Among them, the electron charge states in Si double quantum dots (DQDs) are particularly interested for various reasons such as inherent scalability, existence of a variety of initialization and readout methods, and compatibility with conventional VLSI technologies. When two Si QDs are coupled strongly through a thin tunnel barrier, the molecular states are expected to be formed in the same manner as a hydrogen molecule. On the other hand it was also anticipated that inevitable interaction processes with phonons and photons may corrupt the evolution of the coherent states of the charge qubits and make the decoherence time very short. However, the coherent charge oscillation has been demonstrated successfully for the Si DQDs of about 100 nm in diameter fabricated on the SOI wafer by using the electron beam lithography [6]. The observed decoherence time of beyond 200 nsec is approximately two orders of magnitude longer than those reported for other solid-state qubits based on superconductors and compound semiconductors.

If we scale down the dimension of the Si quantum dots further, we expect that the two-level splitting gets increased and therefore the fundamental qubit frequency is multiplied accordingly. In fact, we have observed the two-level splitting of as large as 0.4 meV at 4.2K for the Si DQDs of 15 - 20 nm in size naturally formed in an ultra-thin nanocrystalline Si film and tunnel-coupled through a ultra-thin grain boundary [7]. The observed splitting is almost one order of magnitude larger than the values reported for GaAs/AlGaAs quantum dots [8]. Fabrication of size-controlled Si DQDs at nanoscale is a challenging issue, and we are currently examining both top-down and bottom-up approaches. As for the bottom-up approach, we succeeded in integrating the nc-Si double nanodots of only 10 nm in diameter deposited by VHF plasma deposition technique [5] onto pre-patterned single-electron transistor (SET) with multiple control gates [9]. The SET was patterned on the heavily-doped SOI using the high-resolution electron beam lithography with a lithographically defined charging island of approximately 90 nm in diameter. The adjacent constrictions, that act as tunnel barriers connecting the charging island to the source and drain leads are of 70 nm in width. The pattern was etched using the ECR-RIE technique and was thermally oxidized at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI down to 30 nm. This leads to the effective dot diameter of approximately 70 nm. After that, a resist hole of only 50 nm square or less was prepared in the gap between the charging island and control gates using the electron beam lithography. The nc-Si dots were then deposited *in-situ*, and the resist was removed from the substrate.

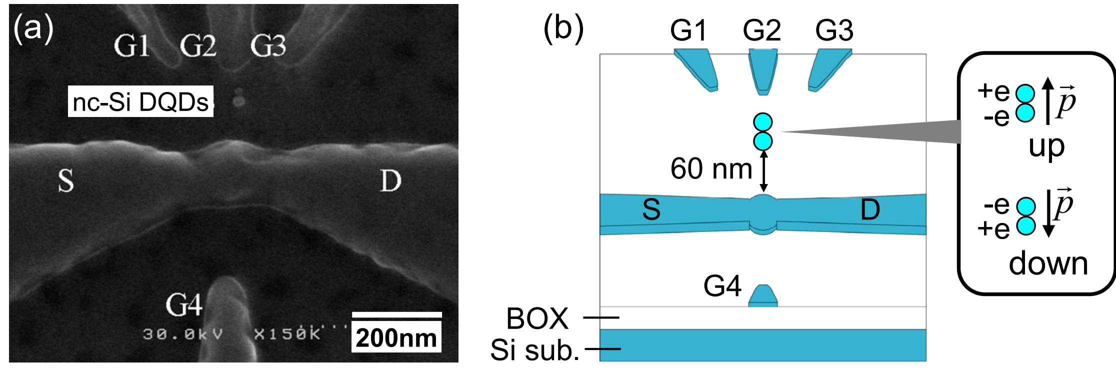

FIG.5 (a) SEM image and (b) a schematic diagram of nanocrystalline Si DQDs integrated with the single-electron transistor

Apparently this process still lacks precision of controlling the number and position of the nc-Si dots in the resist hole, but, for a few devices, we succeeded to have double Si nanodots sitting together as shown in Fig. 5(a). The impact of charge polarization in the fabricated qubit on the tunnelling current through the SET was analyzed by the single-electron circuit simulation with the capacitance parameters obtained by solving 3D Poisson's equation numerically for the device layout (Fig. 5(b)). The calculated results showed that even single-charge polarization with the magnitude of only $\pm e$ can be detected as the remarkable shift of the Coulomb oscillation of the tunnelling current.

Another challenging issue is integrating multiple qubits with a suitable readout device. We need to locate a readout device close enough to the multiple qubits and detect single- or few-electron polarization across them. The readout device should therefore be designed small in its footprint to ensure that the qubit-readout spacing can be downscaled together with the qubit-qubit spacing. For the sake of this, we have recently proposed a compact readout device, where multiple single-electron transistors (SETs) are connected in series [10].

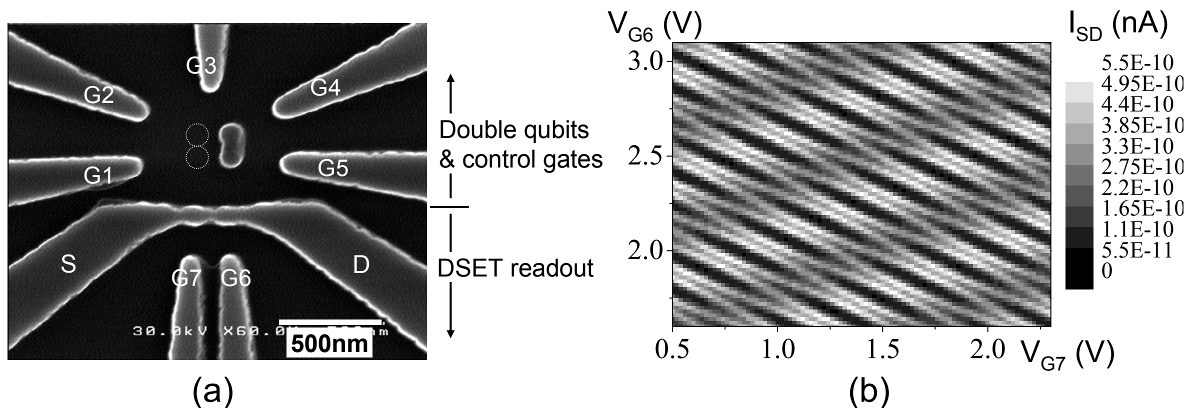

FIG.6 (a) SEM image of a single qubit integrated with the DSET readout device and multiple control gates and (b) simulated tunnel current contour plot as a function of gate voltages, V_{G6} and V_{G7}.

As a demonstrator, a double SET (DSET) readout devcie was fabricated on the SOI substrate by using the same fabrication process as described above. Figure 6(a) shows the SEM image of the DSET with a single qubit patterned simultaneously using the EB lithography. We may also adopt the bottom-up approach for integrating smaller qubits in a similar method as before.

The electrical characteristics for the DSET were measured at 4.2 K and analyzed by using the single-electron circuit simulation. Drain current I_{SD} plotted as a function of two gate voltages, V_{G6} and V_{G7}, showed a clear streamline patten, reflecting the charge stability diagram for tunnel-coupled two charging islands of the DSET. A pair of qubits can take four different single-charge polarization configurations: (left qubit $\vec{p}$, right qubit $\vec{p}$) of (up, down) and (down, up) as energetically-lower configurations and (up, up) and (down, down) as higher ones. We found that these individual charge configurations result in the remarkabke different shifts of the entire current contour pattern, and these shifts can well be utilized to detect the individual charge states of the double qubits.

4. Conclusion

We have overviewed our current attempts to explore the advanced information processing devices in the nanoelectronics domains. For the 'More than Moore' domain, we demonstrated the NEMS memory concept as an examples of co-integrating the heterogeneous nanotechnologies and the conventional silicon nanotechnologies for providing extended device performance and functionalities. Development of such nanotechnologies is expected to be accelerated along with diversification of advanced system applications. On the other hand, no decisive nanodevice technology has been identified for 'Beyond CMOS' domain. We introduced the recent progress of silicon-based quantum information processing technologies where we attempt to highlight the coherent properties of electrons (and their spins) in silicon which are yet to be clarified together with development of the scaling-up technology and practical algorithm suitable for silicon qubits.

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