Single-electron tunnelling via quantum dot cavities built on a silicon suspension nanobridge

Jun Ogi[a,d], Yoshishige Tsuchiya[a,d], Shunri Oda[a,d] and Hiroshi Mizuta[b,c,d]

[a] Quantum Nanoelectronics Research Center, Tokyo Institute of Technology,
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, Japan
Phone: +81-3-5734-2542, FAX: +81-3-5734-2542, e-mail:j.ogi@neo.pe.titech.ac.jp
[b] School of Electronics and Computer Science, University of Southampton,
Southampton Hampshire, UK
[c] Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan
[d]SORST-JST (Japan Science and Technology Agency)

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Recent advance on fabricating Si nano electromechanical systems (NEMS) has enabled us to study single-electron tunnelling through nanometer-scale suspended structures with restrained coupling to the environment [1]. In particular, a suspended quantum dot (QD) cavity structure built on a Si nanobridge (SiNB) provides an ideal system to explore the interaction of single electrons with tailored phonon spectrum in the cavity. Such a system has recently become of great interest in terms of studying physics of decoherence mechanisms for quantum bits and also revealing ultimate energy dissipation process in Si nanostructures. We also expect for such systems new electromechanical phenomena to emerge, which include formation of phononic bandgaps & phonon confinement, phonon blockade [2] and a strong coupling of nanomechanical and electron motions. These phenomena may lead to novel functional Si nano information devices which are not achieved by using the conventional CMOS technologies. In this paper we report on fabrication of SiNB transistor with an integrated QD cavities and characterization of single-electron tunnelling for the first time.

Figure 1 schematically shows structure of a SiNB transistor. In this work we fabricated the SiNB on the SOI wafer by using a SiO_2 (BOX) layer as a sacrificial layer. Figure 2 shows an outline of our fabrication process for SiNB transistors. We first patterned a Si nanowire on a heavily-doped, 50-nm-thick SOI layer by using EB lithography and anisotropic ECR reactive ion etching. After that, we etched the BOX layer isotropically with a liquid HF under the nanowire channel, and a suspended NB channel was formed. The fabricated SiNB transistor is shown in Fig. 3. We conducted thermal oxidation after the NB was patterned in order for making NBs thinner. This enabled us to reduce the width of the NB down to about 15 nm as shown in Fig. 4.

As for integration of QD cavities on the NB, we examined two ways. One is direct patterning the QD cavities with EB lithography. Figure 5 shows the NB with a multiple QD structure patterned by EB lithography. In this process we can locate the multiple QDs to specific places. In the second option, on the other hand, we can introduce a larger number of QDs with smaller dimensions (down to few nm) by employing the heavily-doped nc-Si film grown by using LPCVD on a thermally grown oxide layer. We could use the nc-Si film to form the NBs by applying the same fabrication process to SOI. Figure 6 shows a NB in which many nc-Si dots are embedded naturally in the NB.

We gave lots of care for the rest of the fabrication process as they may damage the formed NB. However, it should be noted that the formed NBs were fairly robust against these post-patterning processes. This is presumably because of the nanometer-scale dimensions of the fabricated NB structures, which receive virtually no friction against a liquid flow in the wet process.

We finally performed electrical measurement of the fabricated SiNB transistors. We characterized the SiNB with single QD cavity on the NBs (see inset of Fig. 7). The SiNB transistor exhibited a clear Coulomb diamond, as shown in Fig. 7. From the measurement results we estimated that gate capacitance C_g is 0.376 aF. This agrees with the theoretical values obtained for the QD geometry in the SiNB transistors by conducing numerical simulation. These results indicate the patterned QD cavity works as a charging island and responsible for the Coulomb oscillation. As a reference we also characterized the devices without underetching the BOX layer (therefore the channel is not suspended), and observed the Coulomb diamond. The tunnel capacitance estimated by the diamonds for these devices are about three times larger than those for the suspended QD devices, for which oxidation proceeds from the all-around surfaces and therefore works to reduce the area of the tunnel junctions more effectively.

[1] J. Ogi *et al*., Abstract of IEEE 2006 Silicon Nanoelectronics Workshop, pp. 123-124 (2006)
[2] E. M. Weig *et al*., Phys. Rev. Lett. **92**, 046804 (2004)

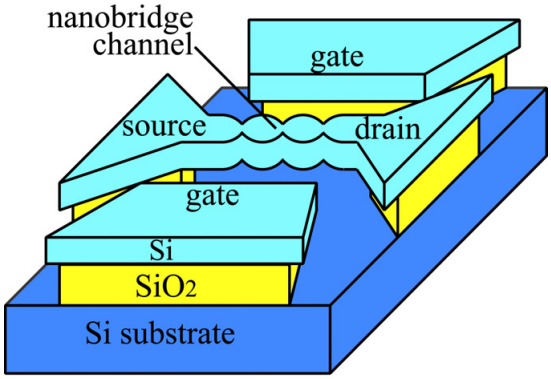

Fig. 1: Device Structure of a SiNB transistor.

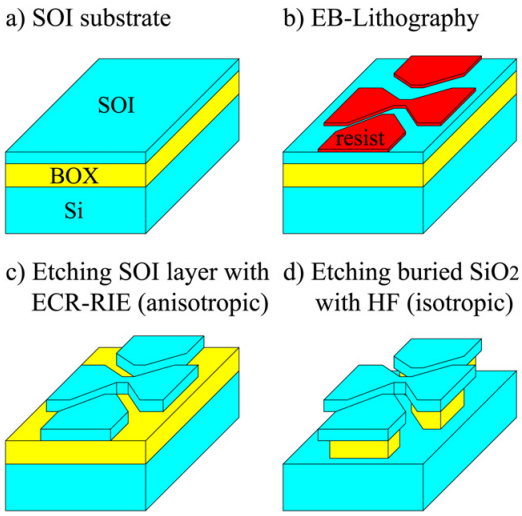

Fig. 2: Fabrication process.

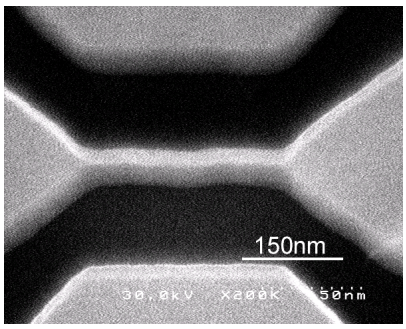

Fig. 3: The SEM image of a fabricated SiNB transistor of 300 nm in length 50 nm in width, taken from an angle of 40°.

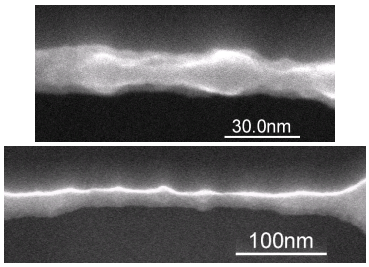

Fig. 4: The narrow SiNB, which was oxidized for 54 minutes at 1000 °C. The bottom image was taken obliquely.

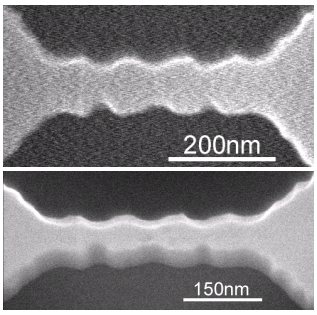

Fig. 5: The SiNB which has multiple QDs patterned by EB lithography. The bottom image was taken obliquely.

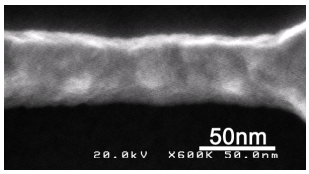

Fig. 6: SEM image of the NB made of nc-Si film. Bright regions in the NB indicate nc-Si grains.

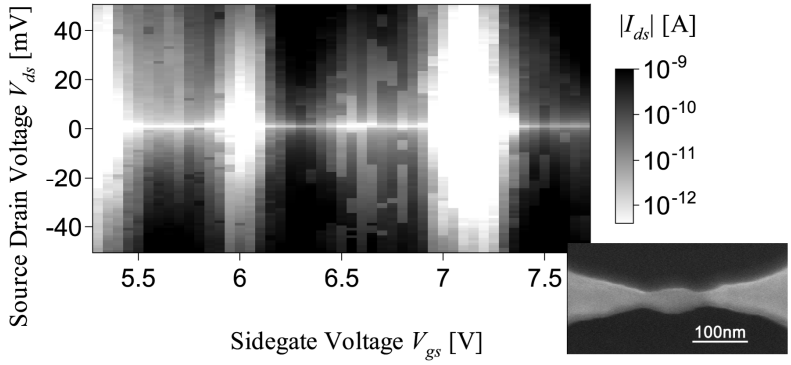

Fig. 7: SET characteristics for the SiNB transistor which has a single QD cavity at temperature of 20 K. The size of the elliptical QD cavity is about 100 nm in the major axis and 35 nm in the minor axis. The inset shows the SEM image of the SiNB.