

Control of electrostatic coupling observed for Si double quantum dot structures

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1. Introduction

In recent years, strongly coupled Si double quantum dot (DQD) structures are attracting much attention as a building unit for quantum information processing. A coherent two level system formed in DQDs has been studied for realizing qubits for the quantum computer [1]. It is vital to control the coupling between DQDs for tuning the two level systems. In this paper we examine controlling the electrostatic coupling in Si DQD structures by using multiple in-plane gates.

2. Fabrication of Si DQD Structures

Si DQD structures connected to the electrodes were fabricated on the heavily-doped silicon on insulator (SOI) of about 40 nm and the buried oxide of 200 nm in thickness. First a 40-nm-thick SOI film, whose thickness was reduced via thermal oxidation at 1100 °C for 75 min, was doped heavily by ion implantation (*n*-type, phosphorous, doping concentration $\sim 1 \times 10^{20} \text{ cm}^{-3}$). DQD structures were then patterned using high-resolution electron beam lithography with the ZEP520A positive resist. Electron cyclotron resonance reactive ion etching was used to transfer the resist pattern onto the SOI layer, and CF_4 was used as etching gas. Thermal oxidation was then done for 30 min or 40 min at 1000 °C to passivate the surface states and to reduce the dot size. Finally, Ohmic contacts were formed by evaporating about 300-nm-thick Al. Figures 1(a) and (b) show SEM images of the device structures, Type A and Type B with different gate structures.

3. Control of Electrostatic Coupling in Si DQD Structures

All measurements were performed at 4.2 K. At first we characterized the Type A device which was oxidized for 30 min at 1000 °C after lithography. The source-drain current (I_{ds}) as a function of voltage applied to Gate 3, where source-drain voltage (V_{ds}) is 2.5 mV, is shown in Figure 2. We observed Coulomb oscillations, which have two different oscillation periods. The long period is about 1.5 V which corresponds to gate capacitance of about 0.1 aF. Figure 3 shows the stability diagram, as a function of voltage for Gate 1 and Gate 3, where V_{ds} is -5 mV. The long period oscillation has random peaks, and the charge triple point is not seen clearly. The origin of the long period oscillation may be multiple islands formed naturally by the potential of random

impurities or defects. On the other hand, the short oscillation period is about 100 mV, which corresponds to gate capacitance of about 1.6 aF. As shown in Figure 4, we observed the charge stability diagram. The short period reflects strong coupling between the gate and the charging island, and the size of the associated charging island should be relatively large, which should be defined by the entire DQD geometry. However the current peak lines are almost in parallel each other. This fact indicates that a single quantum dot is responsible for the current oscillation because the coupling between DQDs is so strong.

Next we characterized the Type B devices. We oxidized the device for 40 min after lithography to decrease coupling between DQDs. Figure 5(a) shows the DQD stability diagram as a function of voltage for Gate 2 and Gate 3 where V_{ds} is 0.2 mV. We observed the DQD characteristics successfully by optimizing the DQD dimensions and oxidation conditions. We then tuned the voltage for Gate 1 for controlling the electrostatic coupling. We applied the voltage for Gate 1 of (b) -100 mV and (c) -200 mV. As shown circle on the Figure 5, the boundary of the hexagonal regions (indicated by an open circle) gradually disappears, and the triple points become relatively clear with increasing negative voltage for Gate 1. This is attributable to the electrostatic potential barrier induced by Gate 1, and the electrostatic coupling between DQDs became weaker.

4. Summary

We fabricated two types of Si DQD structures and characterized them. DQD property was observed by using optimized structure and oxidation condition. Electrostatic coupling between DQDs was found controllable with the side gate.

Acknowledgment

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Reference

- [1] J. Gorman, *et al.* Phys. Rev. Lett. **95**, 090502 (2005)

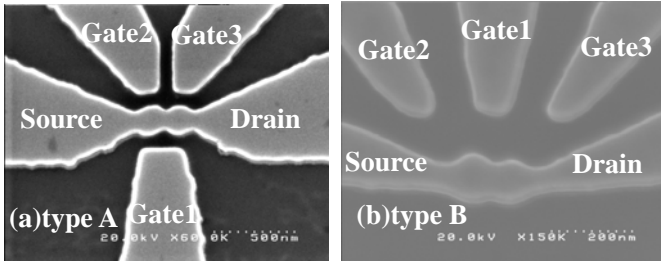


Figure 1: SEM images of two types of Si double quantum dots structure.

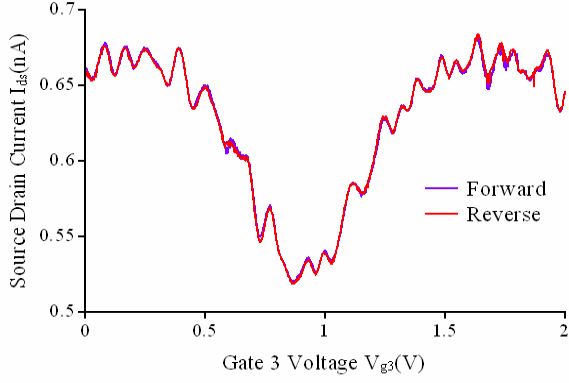


Figure 2: Source-drain current I_{ds} with Gate 3 voltage V_{g3} of device type A at 4.2 K. Source-drain bias V_{ds} is 2.5 mV.

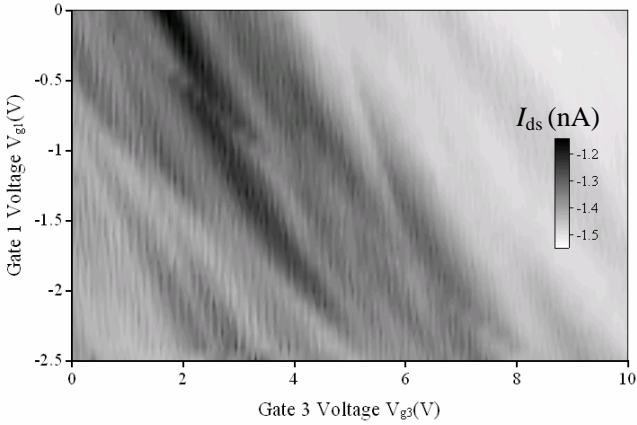


Figure 3: Stability diagram with Gate 1 and Gate 3 of device type A at 4.2 K. Source-drain bias V_{ds} is -5 mV.

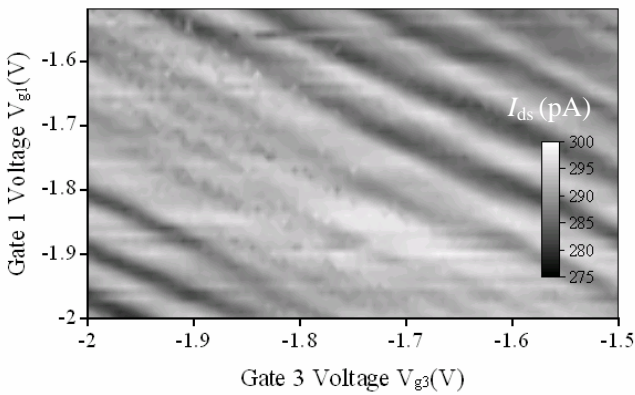


Figure 4: Stability diagram with Gate 1 and Gate 3 of device type A at 4.2 K. Source drain bias V_{ds} is 1 mV.

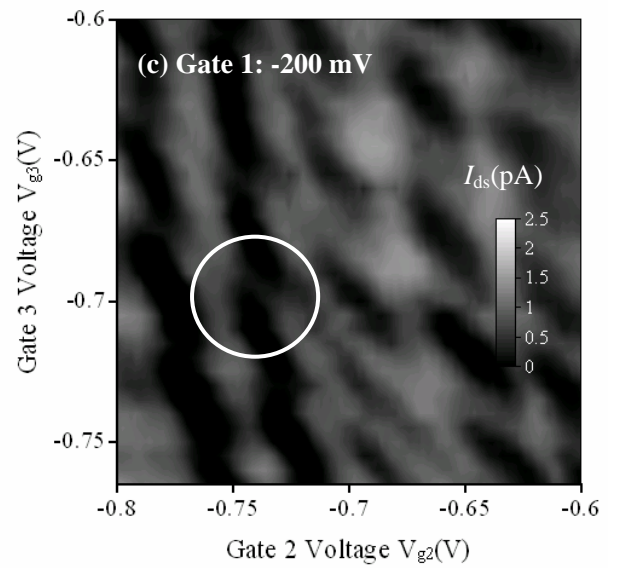
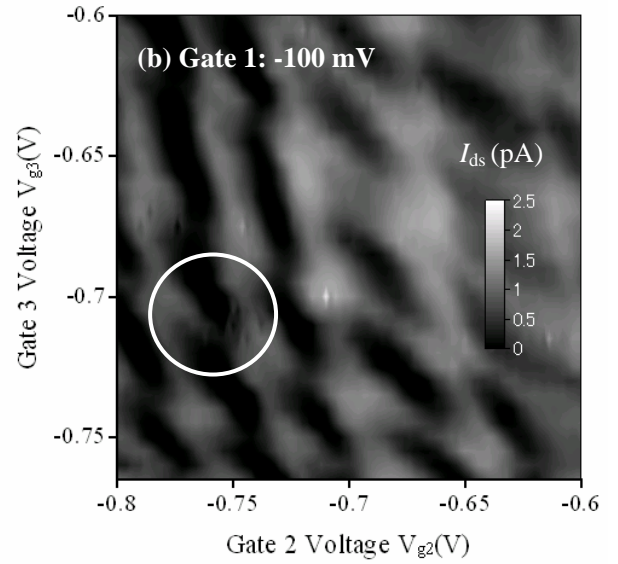
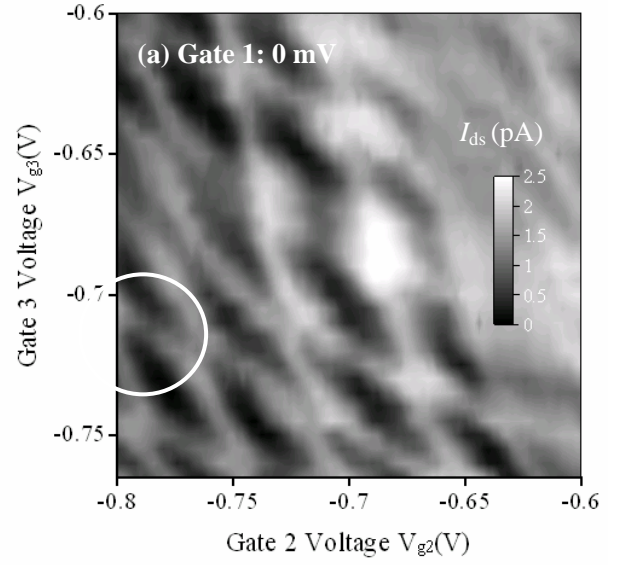


Figure 5: Stability diagram with Gate 2 and Gate 3 of device type B at 4.2 K. Source drain bias V_{ds} is 0.2mV. Gate 1 voltages are (a):0 mV, (b):-100 mV, (c):-200 mV.