

Study of Single-Charge Polarization on two Charge Qubits Integrated onto a Double Single-Electron Transistor Readout

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1. Introduction

Solid-state approach offers the promising way to integrate a large number of quantum bits (qubits) to realize quantum computers. Double Quantum Dots (DQDs) have been extensively studied as a candidate for the charge qubit. Early DQD research has been done for GaAs/AlGaAs hetero-structures [1], but silicon based DQDs have recently been fabricated using the top-down fabrication technique, and a long decoherence time has been demonstrated [2]. Silicon based DQDs are also preferred because of their compatibility with the existing silicon fabrication process. Decoherence time of the qubit should be extended further for accomplishing fault tolerant quantum computation. It has also been studied to adopt nanocrystalline Si DQDs deposited by VHF plasma deposition technique for realizing extremely downscaled charge qubits [3].

Another key issue is to integrate multiple charge qubits with a suitable readout device. We recently proposed multiple single-electron transistors (MSETs) [4], where SETs are connected in series, for sensing single-charge polarization over the multiple qubits. In this paper we fabricate and evaluate a double single-electron transistor (DSET) (Fig. 1) to clarify the readout scheme. In the DSET configuration, qubits operation is controlled via electrodes (G3-G7), and the gate electrodes G1 and G2 are used to manipulate the electrochemical potentials on the SET islands. We demonstrate how different single-charge configurations on a pair of DQDs are sensed by using the DSETs by using the measured electrical characteristics for the DSET and the equivalent circuit simulation.

2. Fabrication of DSETs

DSET was fabricated on the phosphorus doped ($\sim 10^{19}$ cm⁻³) silicon-on-insulator (SOI) substrate with BOX thickness of 200nm. SEM image of fabricated DSET without qubits and with qubits are shown in Fig. 1(a) and Fig. 1(b), respectively. Lithographically defined diameter of the each island was 90 nm and pattern was transferred to SOI by using the electron cyclotron resonance-reactive ion etching (ECR-RIE) technique. At this fabrication process, thickness of the SOI layer is 40 nm. After etching, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI down to 30 nm. This leads to the resulting overall dot diameter of approximately 45 nm. In this device structure, adjacent constrictions act as tunnel barriers connecting the charging islands to the

source and drain electrodes.

3. Electrical characteristics for DSETs

Electrical measurements were carried out at 4.2 K for the fabricated DSET without qubits. Figure 2 and Figure 3 show the contour plots of differential conductance ($\partial I_D / \partial V_D$) as a function of V_{G1} , V_D and V_{G2} , V_D , respectively. Clear Coulomb blockade with different Coulomb diamond sizes can be observed in both the plots. This confirms the presence of the two islands in the fabricated structure. Contour plot of I_D as a function of V_{G1} and V_{G2} is shown in the Fig. 4 for the drain voltage of 500 μ V. From this contour plot, it can be understood that number of electrons in each of the SET can be controlled individually by the gate potentials. The equivalent circuit of DSET is shown in Fig. 5 (a). Equivalent circuit capacitance values $C_{G1I1}=0.52$ aF (G1-Island 1), and $C_{G1I2}=0.38$ aF (G1-Island 2), $C_{G2I1}=0.75$ aF (G2-Island 1), $C_{G2I2}=1.05$ aF (G2-Island 2) were extracted from the contour plot of the gates G1 and G2.

4. Readout of single-charge polarization on two qubits

To characterize the effect of charge polarizations in a pair of DQDs on the DSET, equivalent circuit simulation was done at 4.2 K. The equivalent circuit of the DSET with DQDs is shown in Fig. 5 (b). Figures 6(a) and 6(b) show the simulation results for charge configurations of DQDs shown in the inset figures. Triple points in Fig. 6 (b) are shifted toward right bottom direction from those points in Fig. 6 (a). It indicates that change in polarizations in the pair of DQDs shift contour plot characteristics remarkably. Effects of the various polarization condition on DSET can be easily understood from the drain current characteristics as a function of V_{G2} at $V_{G1}=1.0$ V shown in Fig. 6 (c).

5. Conclusions

We fabricated DSET to detect single-charge polarization on a pair of qubits independently. Operation of the individual SETs was successfully demonstrated, and the electrical characteristics measured for the DSET were validated by comparing with the equivalent circuit simulations. We also demonstrated that charge polarizations on the pair of qubits could be distinguished by using the adjacent DSET.

References

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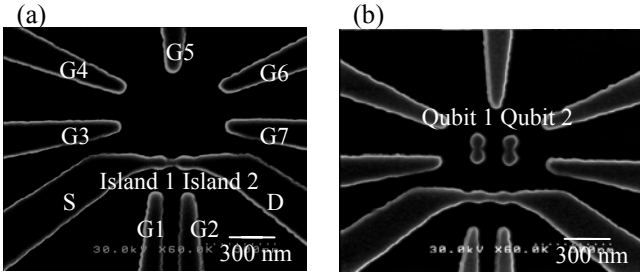


Fig. 1 SEM image of DSETs and qubits gates: (a) without qubits; (b) with qubits.

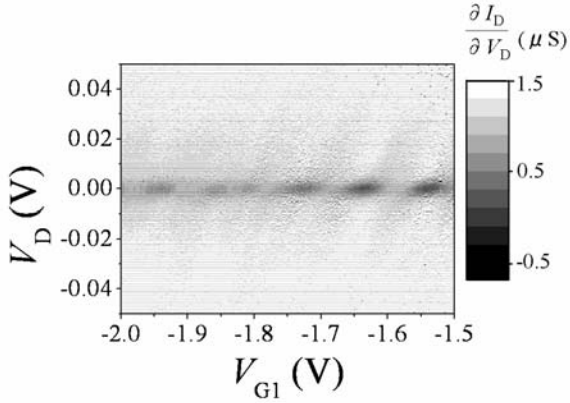


Fig. 2 Contour plot of the measured differential conductance ($\partial I_D/\partial V_D$) as a function of V_{G1} and V_D at 4.2 K.

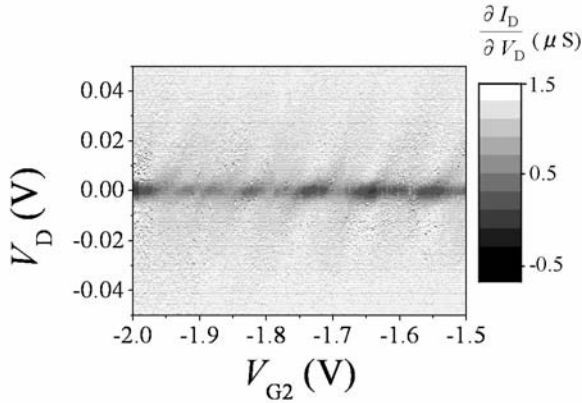


Fig. 3 Contour plot of the measured differential conductance ($\partial I_D/\partial V_D$) as a function of V_{G2} and V_D at 4.2 K.

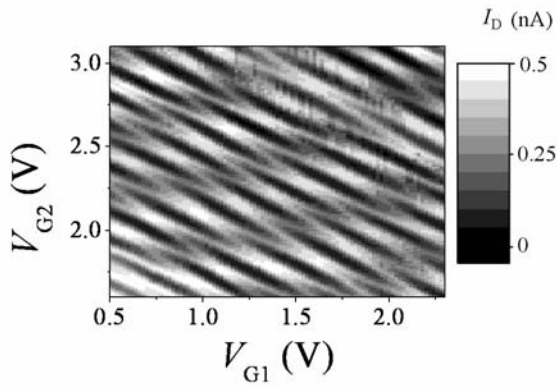


Fig. 4 Contour plot of the measured I_D as a function of V_{G1} and V_{G2} with $V_D = 500 \mu\text{V}$ at 4.2 K.

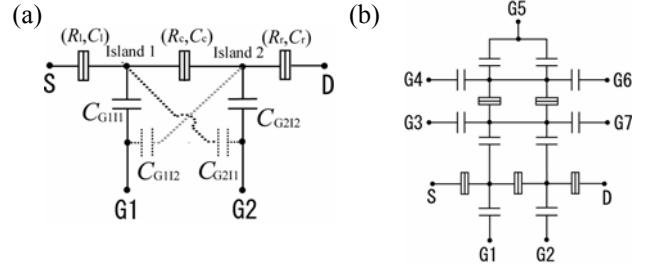


Fig. 5 Equivalent Circuits of (a) DSET; (b) DSET with qubits. Cross capacitances are abbreviated for clarity.

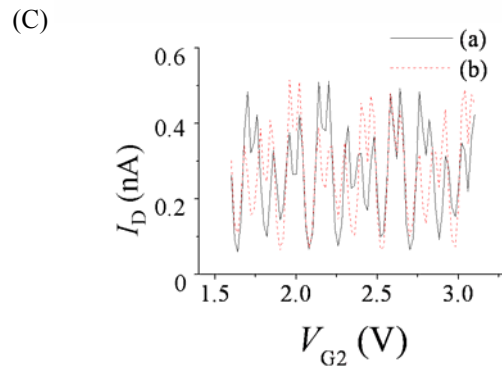
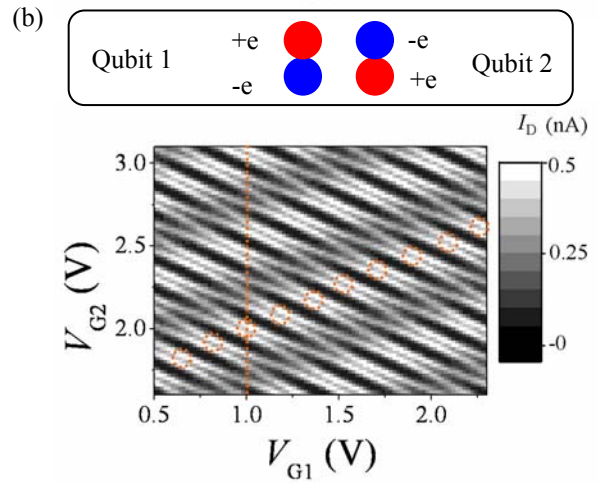
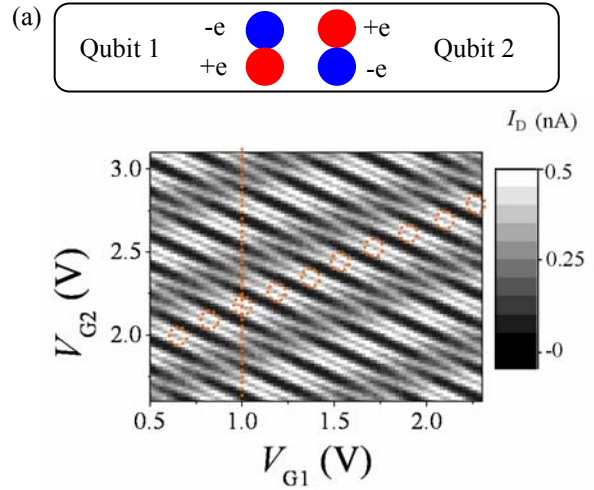


Fig. 6 (a), (b): Contour plots of the simulated I_D as a function of V_{G1} and V_{G2} with $V_D = 500 \mu\text{V}$ at 4.2 K for the charge polarizations shown in inset figures. (c) I_D - V_{G2} at $V_{G1} = 1.0 \text{ V}$ shown as dotted lines in (a) and (b).