

Frontier Process 2007
17 August 2007

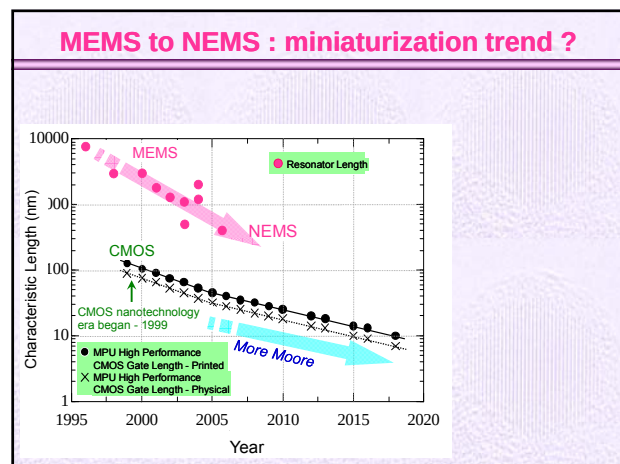
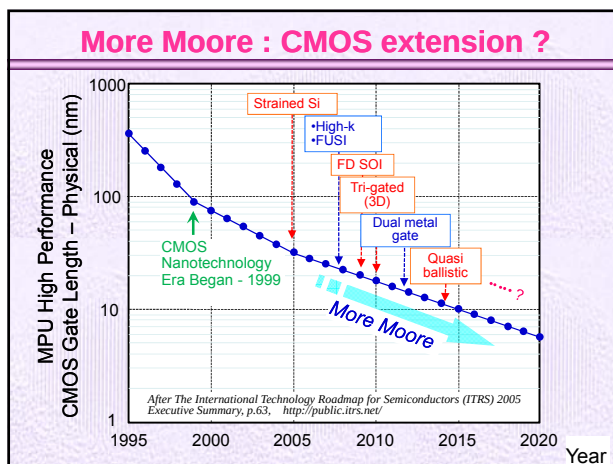
Functional silicon nanoelectro-mechanical information processing devices

H. MIZUTA
School of Electronics & Computer Science, Univ. of Southampton
Department of Physical Electronics, Tokyo Inst. Technology
SORST JST (Japan Science and Technology)

Y. Tsuchiya, S. ODA
Quantum Nanoelectronics Res. Centre, Tokyo Tech.
SORST JST (Japan Science and Technology)

OUTLINE

1. Introduction – Integration of nano electro-mechanical (NEM) structures into Si devices for information processing
2. NEM nonvolatile memory
3. NEM single-electron devices
4. Summary



Progressing high-speed Si based MEMS

1996

Si beam
 $L = 7.7 \mu\text{m}$
 $t = 0.33 \mu\text{m}$
 $h = 0.8 \mu\text{m}$
 $f_R = 70.72 \text{ MHz}$

2003

3C-SiC beam
 $L = 1.1 \mu\text{m}$
 $w = 120 \text{ nm}$
 $h = 75 \text{ nm}$
 $f_R = 1 \text{ GHz}$

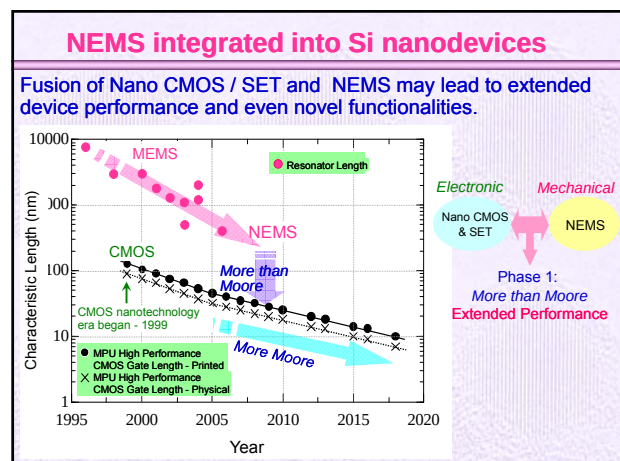
Oscillation frequency of a doubly clamped beam

$$\omega_n \propto \frac{t}{L^2}$$

L : beam length
 t : beam thickness

X.M.Henry Huang *et al.*,
Nature **421**, 496 (2003).

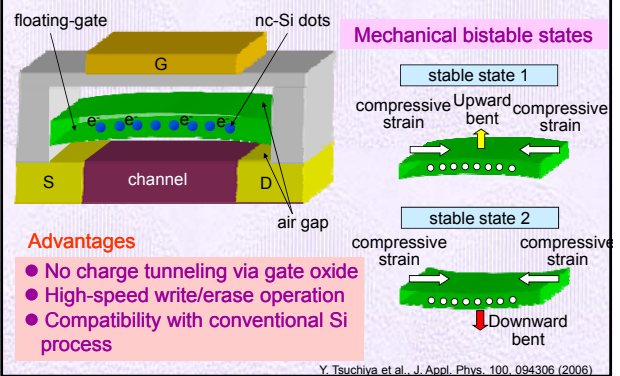
Over 1 GHz operation possible with size reduction



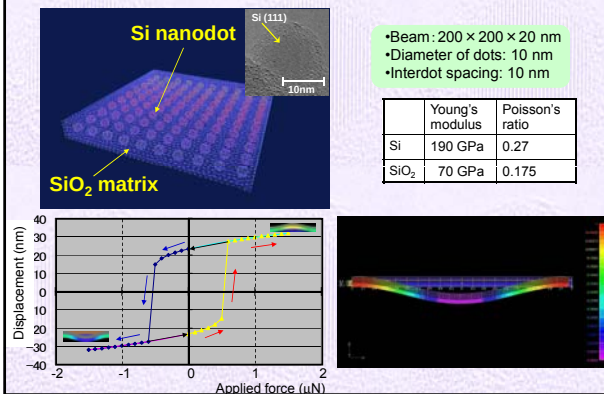
OUTLINE

1. Introduction – Integration of nano electro-mechanical (NEM) structures into Si devices for information processing
2. NEM nonvolatile memory

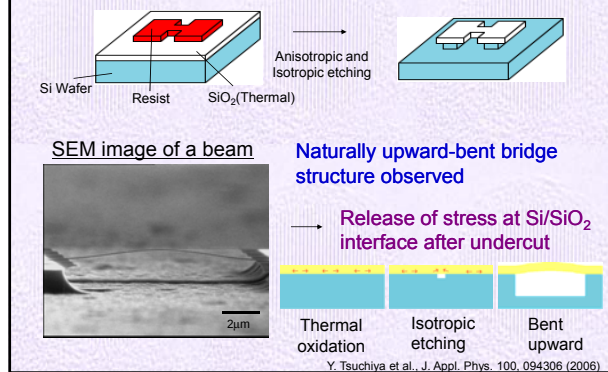
Nonvolatile NEM memory



Buckled SiO₂ beam with embedded SiNDs

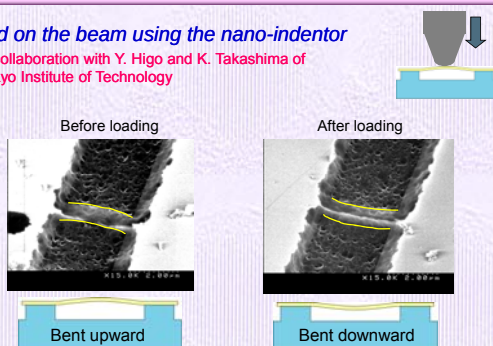


Test beam structure fabrication

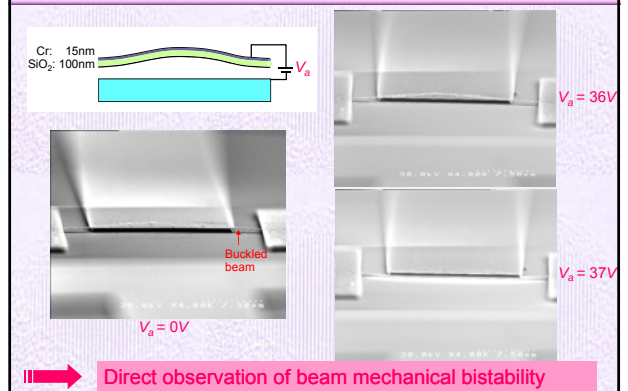


Loading experiment for the beam

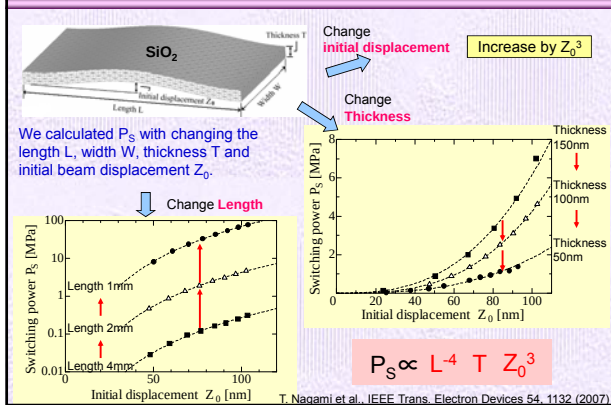
Load on the beam using the nano-indenter
in collaboration with Y. Higo and K. Takashima of Tokyo Institute of Technology



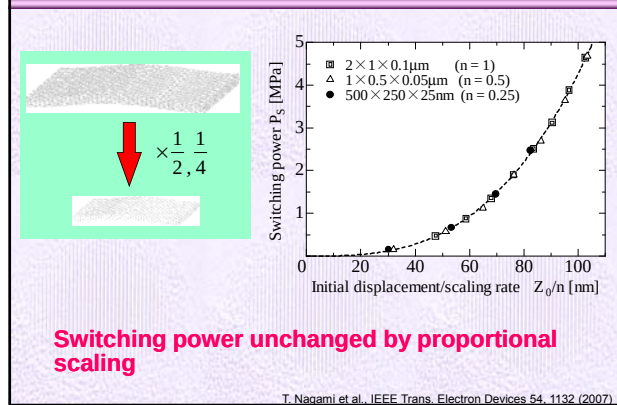
Electrical switching of the beam



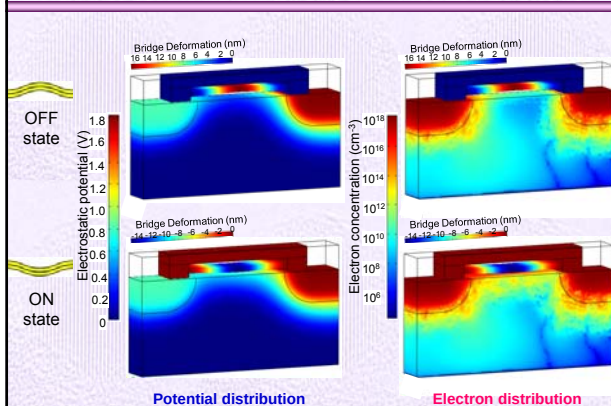
Mechanical properties of buckled FG



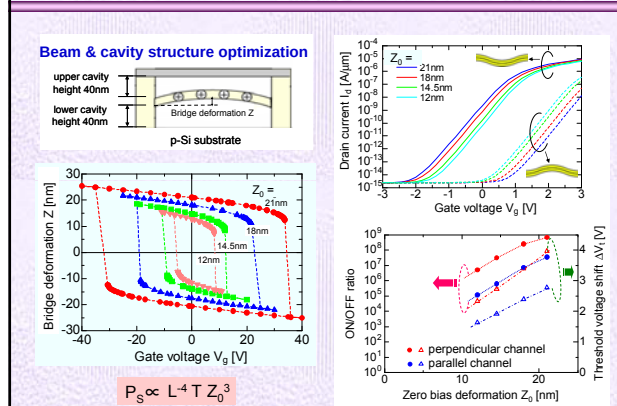
Scaling law for switching power



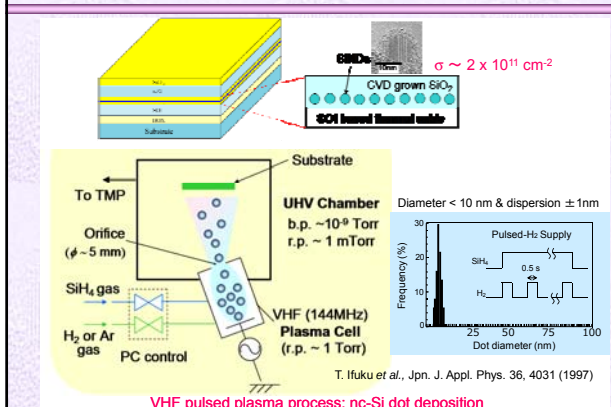
Readout operation of NEM memory



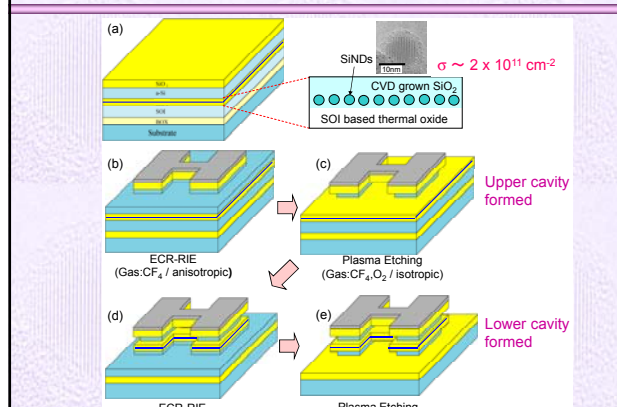
Optimized Readout characteristics



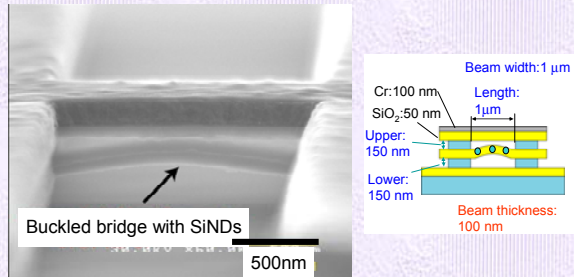
Fabrication of FG with SiNDs



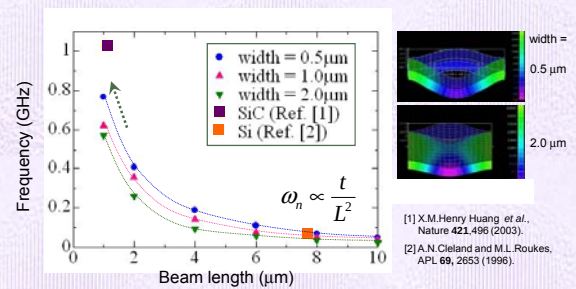
Fabrication of FG with SiNDs



Fabrication of FG with SiNDs

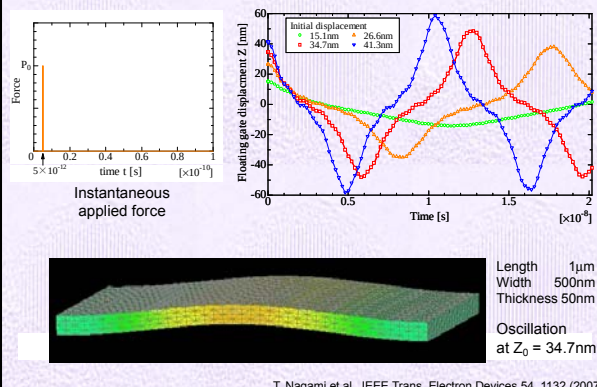


Switching speed of a simple flat FG

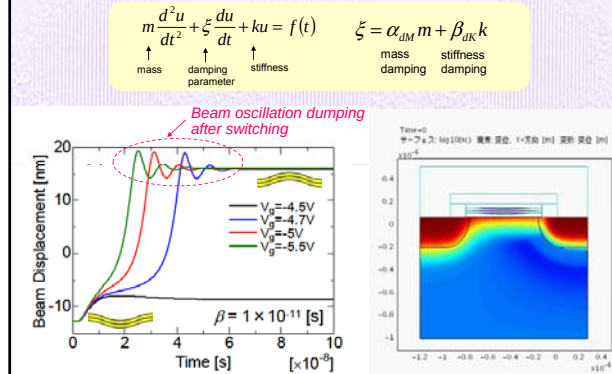


For a simple flat SiO₂ beam with $L < 1 \mu\text{m}$, over 1GHz frequency can be obtained, but.....

Switching speed of a buckled bistable FG



Beam damping effects on switching speed



A variety of nonvolatile RAM candidates

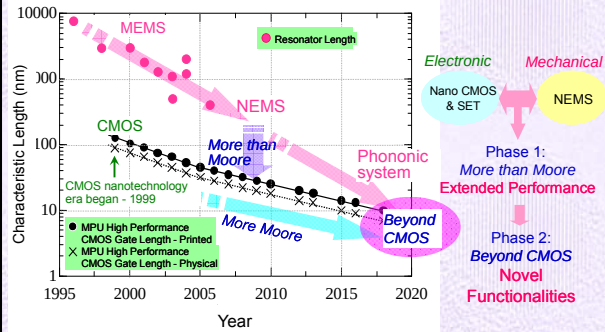
	Cell	Flash	Nano-Crystal	FeRAM	PCRAM	MRAM	NEM Memory
Device Structure							
Mechanism of Non-volatility		Charge in Floating Gate	Charge in Nano-dot	Polarization	Phase Change	MR Change	Mechanical bistability
Issues		Program Volt. reduction	Program Volt. reduction	H ₂ block CVD	Program Curt. reduction	Program Curt. reduction	Power reduction, Shock immunity
Cell Size		4-8 F ²	4-8 F ²	10-20 F ²	8-15 F ²	8-15 F ²	6-10 F ²
Program		10 μs	10 μs	<50 ns	100 ns	<50 ns	<50 ns
Read		<20 ns	<20 ns	100 ns	<20 ns	<50 ns	<20 ns ?
Voltage		< 12 V	< 12 V	5 V	3 V	3 V	< 10V
P/E Cycle		10 ⁸	10 ⁸	10 ¹⁰	10 ¹²	10 ¹⁵	> 10 ¹² ?

OUTLINE

1. Introduction – Integration of nano electro-mechanical (NEM) structures into Si devices for information processing
2. NEM nonvolatile memory
3. NEM single-electron devices

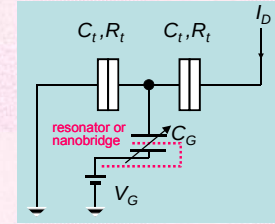
What can we explore in 'real' NEMS ERA?

Fusion of Nano CMOS / SET and NEMS may lead to extended device performance and even novel functionalities.



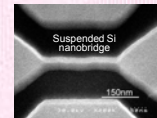
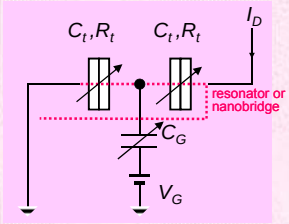
Fusion of NEMS & single-electron transistors

SET-NEMS

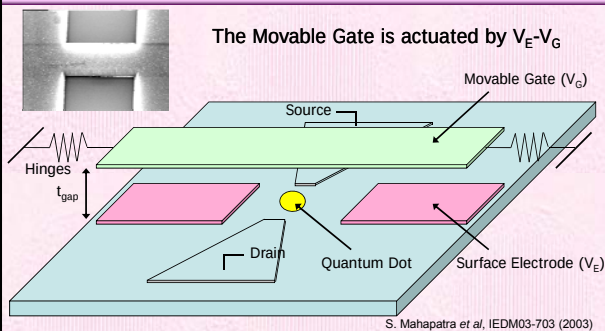


M.D. Lahaye et al., Science 304, 74 (2004)

NEMSET

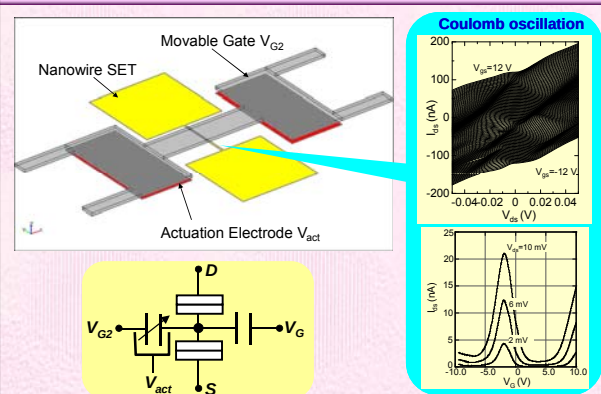


Concept of SET-NEMS: movable gate SET

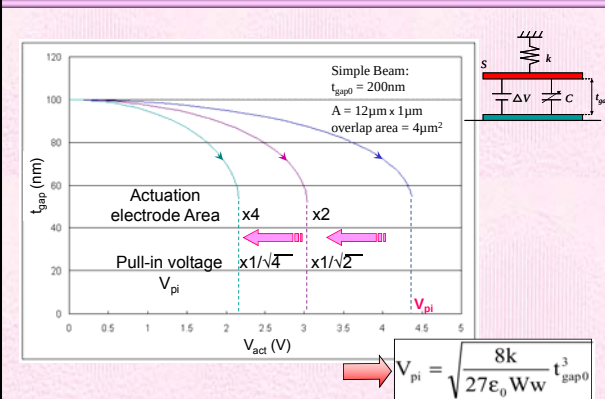


♦ The design of the movable gate in a 3-D context is essential to achieve the expected performance.

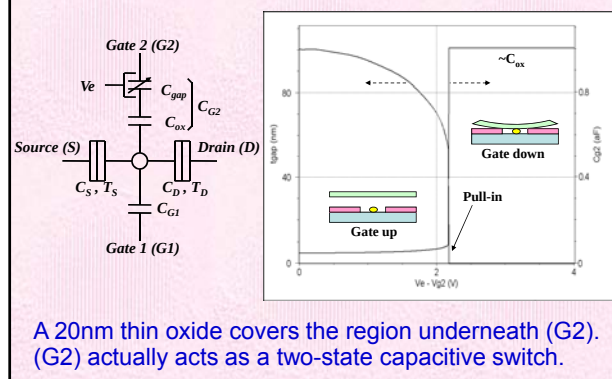
SET-NEMS: extended functionalities to SETs



Pull-in operation of movable gate

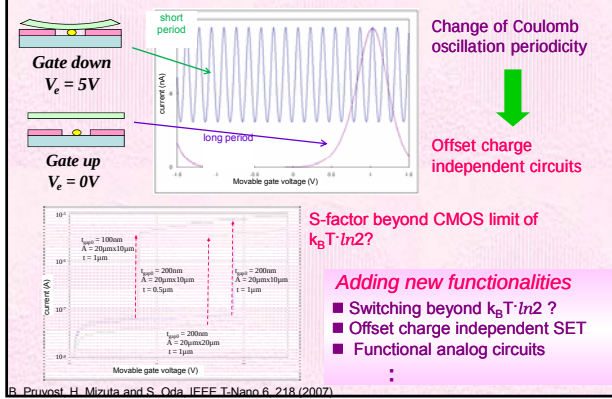


Two-state capacitive switch

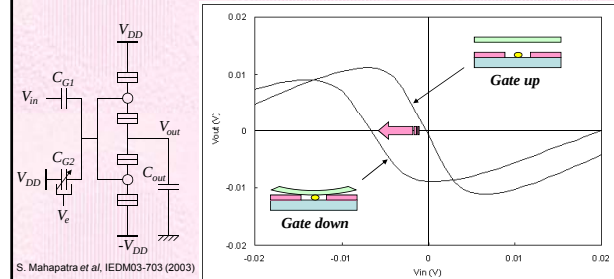


A 20nm thin oxide covers the region underneath (G2). (G2) actually acts as a two-state capacitive switch.

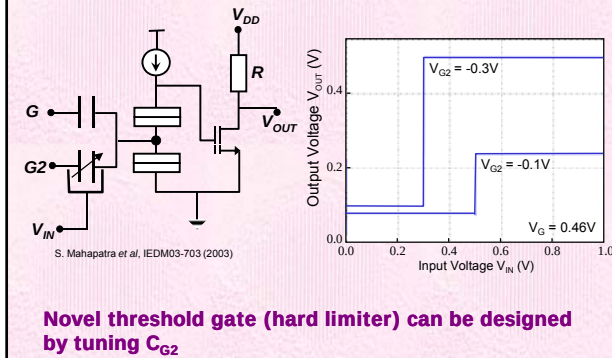
Unique switching properties of SET-NEMS



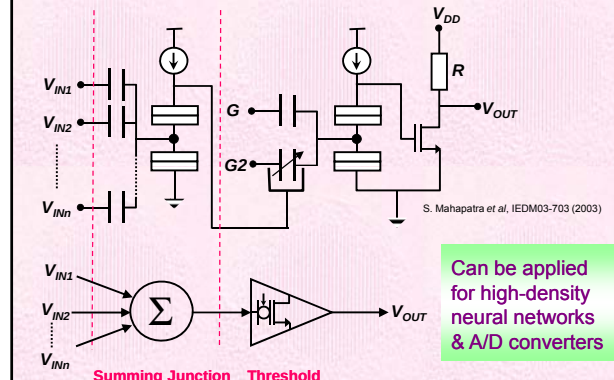
Tunable threshold SET inverter



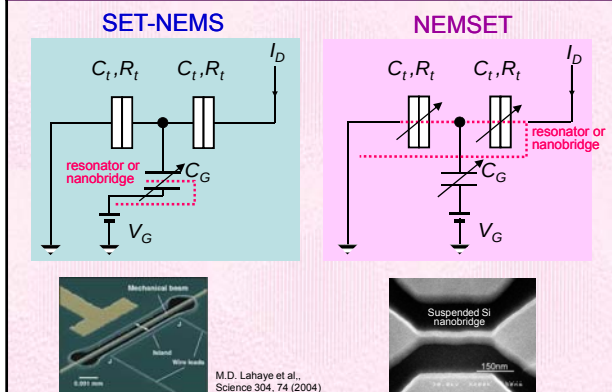
SETMOS-NEMS as a novel threshold gate



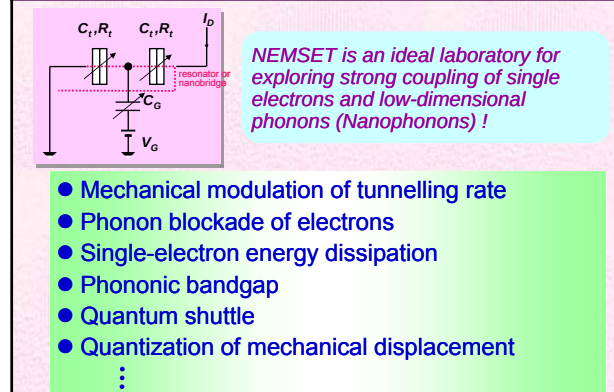
SETMOS-NEMS based hybrid neuron cell

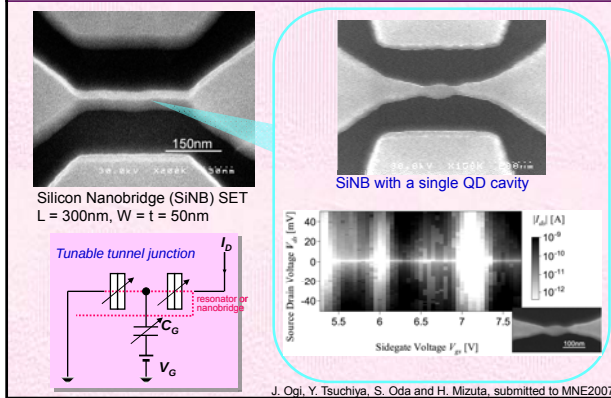
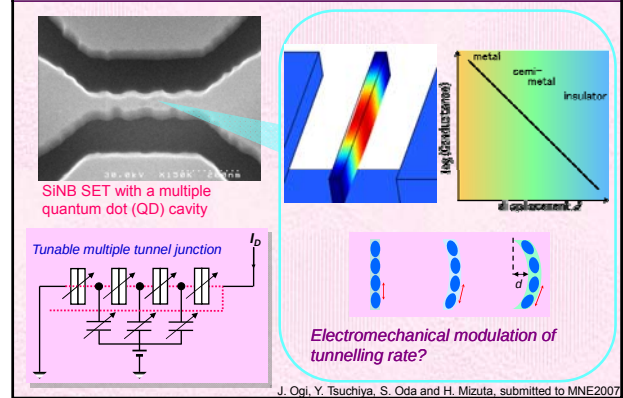
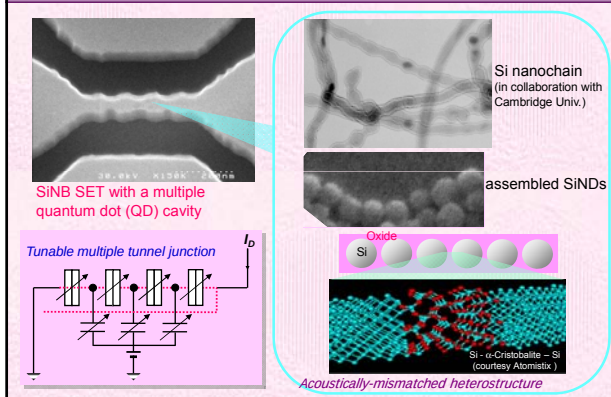
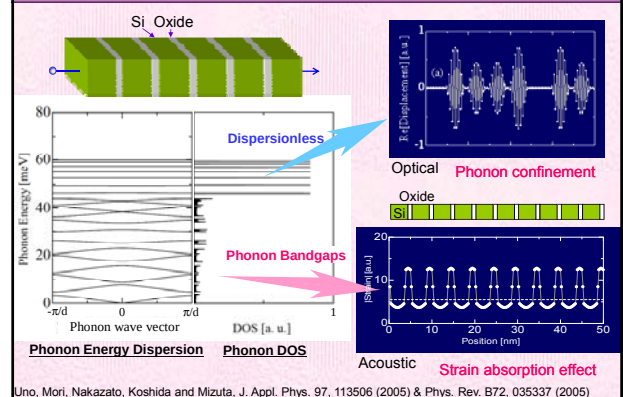
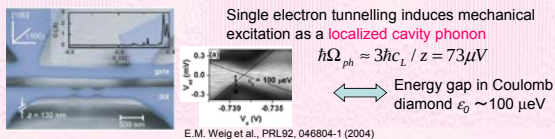
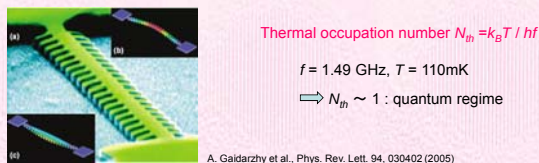
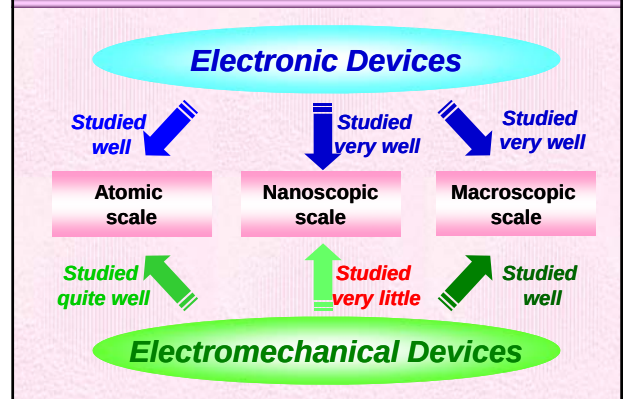


Fusion of NEMS & single-electron transistors



NEMSET: strongly-coupled electron-phonon system



NEMSET(1): Mechanically modulated tunnelling rate**NEMSET(1): Mechanically modulated tunnelling rate****NEMSET(1): Mechanically modulated tunnelling rate****NEMSET(2): Phononic bandgap formation****NEMSET(3): Even more exotic phenomena****Phonon blockade of single-electron tunnelling****Quantization of mechanical motion?****Nanoscale EM phenomena unexplored!**

SUMMARY

- Fusion of Si nanodevice and NEMS may provide enhanced performance and even new functionalities to 'conventional' Si devices for information processing
- NEM memory with high-speed operation & superior nonvolatility: any chance to compete with other emerging memories?
- SET-NEMSs and NEMSETs with more functionalities and new switching principle: still lots of space to explore !!

Acknowledgement

- Tokyo Institute of Technology
T. Nagami, B. Pruvost, J. Ogi, S. Matsuda,
J. Shibamura, S. Sawai,
K. Takai and N. Momo (now of Toshiba Co.)
- University of Cambridge
W. I. Milne, Z.A.K. Durrani
- Hitachi Central Research Laboratory
S. Saito, T. Arai, H. Fukuda, T. Onai, T. Shimada
- Nagoya University
S. Uno