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&
Department of Physical Electronics, Tokyo Institute of Technology

**Quantum Nanoelectronics Research Center,
Tokyo Institute of Technology**

1. Introduction – Co-integration of NEMS with silicon devices for information processing
2. Bistable NEMS based memory devices
3. Other NEMS memory
4. Summary

1. Introduction – Co-integration of NEMS with silicon devices for information processing

Figure 1 is a log-linear plot showing the characteristic length (nm) of various semiconductor technologies over time (Year). The y-axis is logarithmic, ranging from 1 nm to 10,000 nm. The x-axis is linear, ranging from 1995 to 2020. The plot illustrates the progression of Moore's Law and the end of transistors.

The data series include:

- Resonator Length (pink circles):** Shows a rapid decrease in length, following Moore's Law (dashed line) until approximately 2005, after which it diverges upwards.
- CMOS Gate Length - Printed (black dots):** Shows a steady decrease in length, following Moore's Law (dashed line) until approximately 2015, after which it diverges upwards.
- CMOS Gate Length - Physical (green crosses):** Shows a steady decrease in length, following Moore's Law (dashed line) until approximately 2010, after which it diverges upwards.

Key annotations include:

- A green arrow pointing to the year 1999, labeled "CMOS nanotechnology era began - 1999".
- A blue arrow pointing to the year 2015, labeled "More Moore".
- Labels for "MEMS" (pink) and "NEMS" (pink) are placed near the Resonator Length data points.
- A label for "CMOS" (green) is placed near the CMOS Gate Length - Printed data points.

A.N.Cleland and M.L.Roukes
Appl.Phys.Lett. **69**, 2653 (1996).

$$\omega_n \propto \frac{t}{L^2}$$

L : beam length
 t : beam thickness

X.M.Henry Huang *et al.*,
Nature **421**,496 (2003).

Over 1 GHz operation possible with size reduction

The figure is a semi-log plot showing the characteristic length (nm) on the y-axis (log scale from 1 to 1000) versus the year on the x-axis (linear scale from 1995 to 2020). The plot tracks the scaling of various technologies:

- MEMS (pink dots):** Resonator Length, showing a trend from ~1000 nm in 1995 to ~300 nm in 2010.
- NEMS (pink dots):** Resonator Length, continuing the trend from ~300 nm in 2010 to ~10 nm in 2018.
- CMOS (black dots and crosses):**
 - MPU High Performance (black dots):** Gate Length, showing a trend from ~100 nm in 1995 to ~10 nm in 2018.
 - CMOS Gate Length - Printed (black crosses):** Following a similar trend to the MPU high performance gate length.
 - MPU High Performance CMOS Gate Length - Physical (black crosses):** Following a similar trend to the MPU high performance gate length.
- Phononic system (pink arrow):** Indicated as a future technology path.

Annotations and trends:

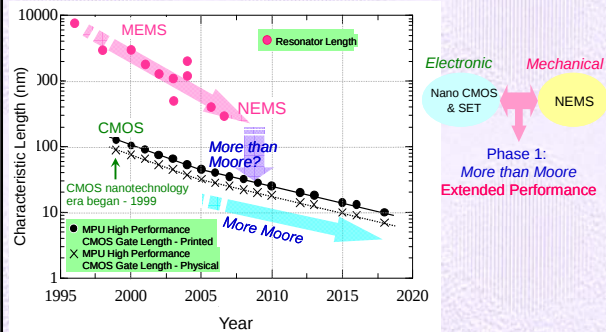
- CMOS nanotechnology era began - 1999:** Marked by an arrow pointing to the start of the CMOS data series.
- More Moore?:** A blue arrow pointing to the right, indicating continued scaling.
- Beyond CMOS?:** A pink oval highlighting the region where the characteristic length approaches 10 nm.

Diagram on the right:

- Electronic:** Nano CMOS & SET.
- Mechanical:** NEMS.
- Phase 1:** More than Moore Extended Performance (indicated by a pink arrow from Electronic to Mechanical).
- Phase 2:** Beyond CMOS Novel Functionalities (indicated by a pink arrow from Phase 1).

NEMS integrated into Si nanodevices

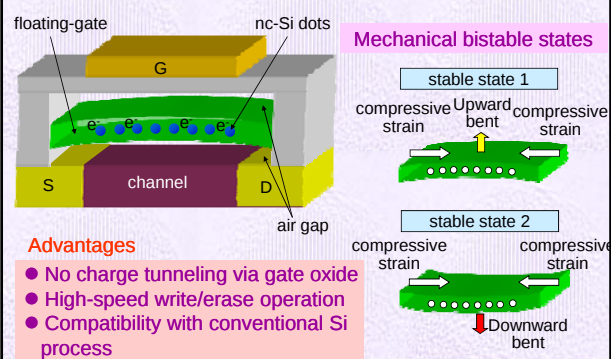
Fusion of Nano CMOS / SET and NEMS may lead to extended device performance and even novel functionalities.



OUTLINE

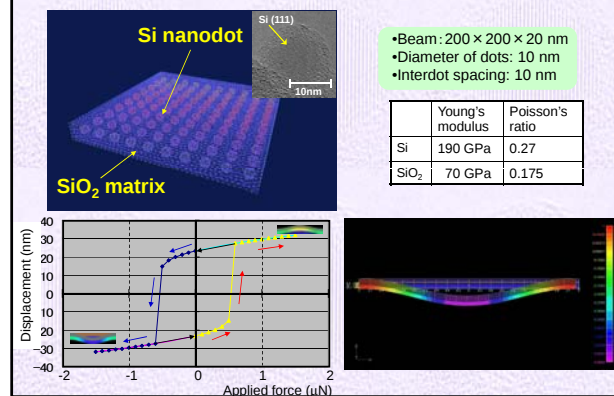
1. Introduction – Co-integration of NEMS with silicon devices for information processing
2. Bistable NEMS based memory devices

Nonvolatile NEM memory

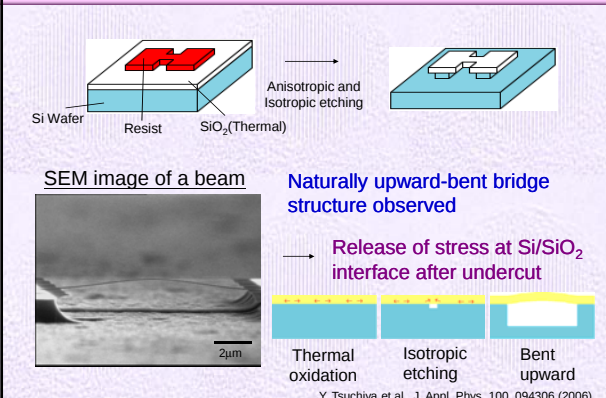


Y. Tsuchiya et al., J. Appl. Phys. 100, 094306 (2006)

Buckled SiO₂ beam with embedded SiNDs



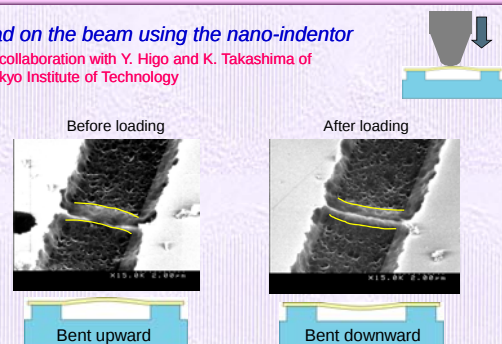
Test beam structure fabrication



Y. Tsuchiya et al., J. Appl. Phys. 100, 094306 (2006)

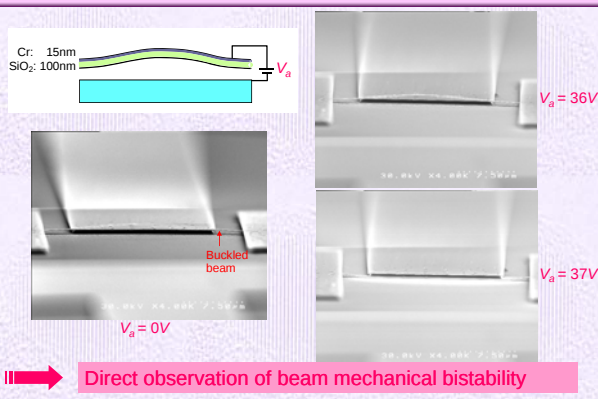
Loading experiment for the beam

Load on the beam using the nano-indenter
in collaboration with Y. Higo and K. Takashima of Tokyo Institute of Technology



Y. Tsuchiya et al., J. Appl. Phys. 100, 094306 (2006)

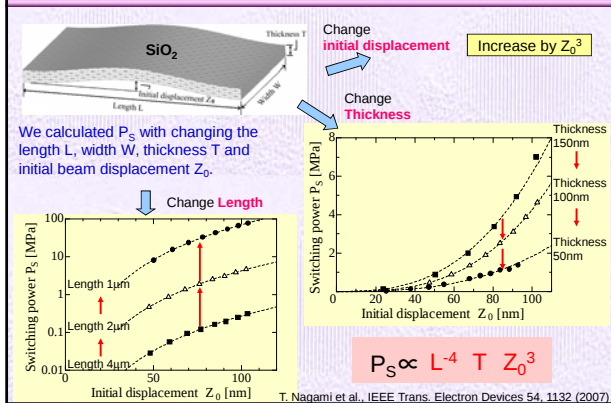
Electrical switching of the beam



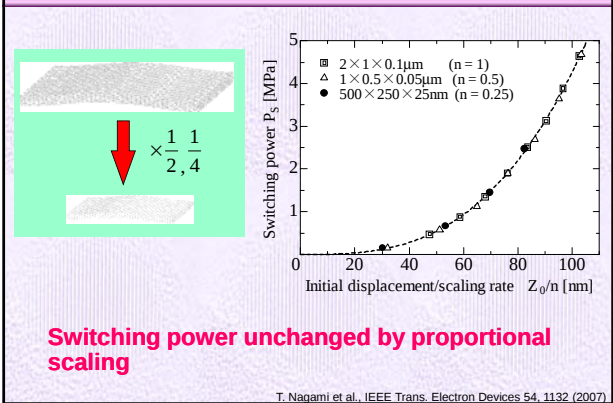
Japanese mechanical bistable device 200 years ago



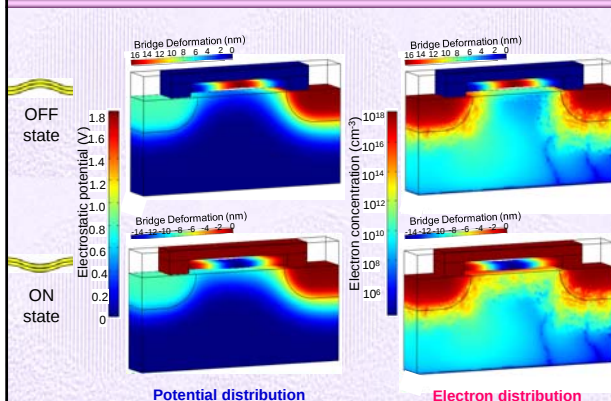
Mechanical properties of buckled FG



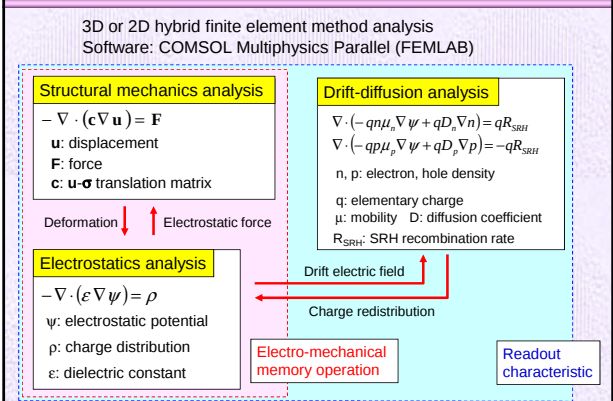
Scaling law for switching power



Readout operation of NEMS memory



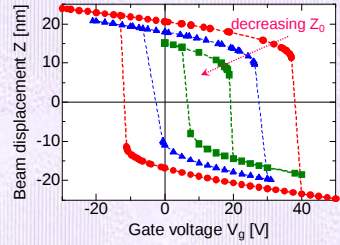
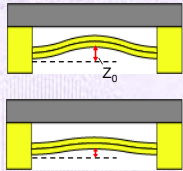
Hybrid electromechanical – transport simulation



For reducing switching voltage

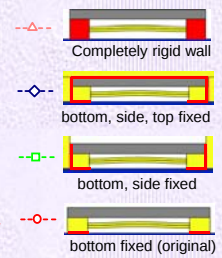
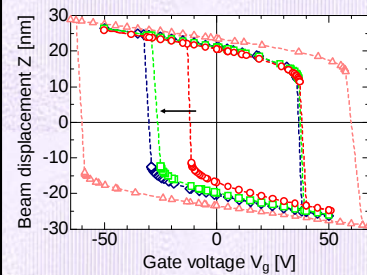
$$P_S \propto L^{-4} T Z_0^3$$

Smaller zero bias displacement leads to lower switching voltage



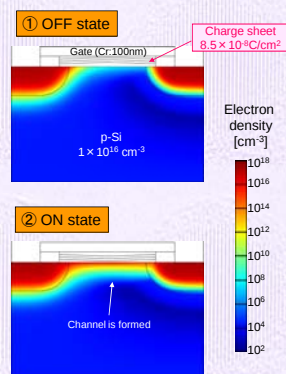
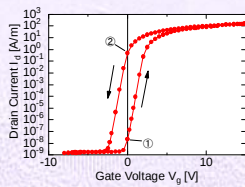
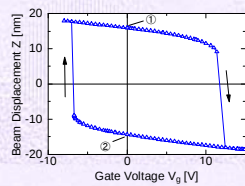
Simple reduction of Z_0 may result in losing bistability.

Effects of cavity structures



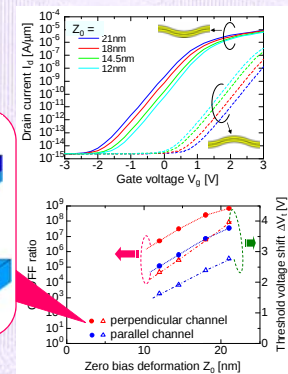
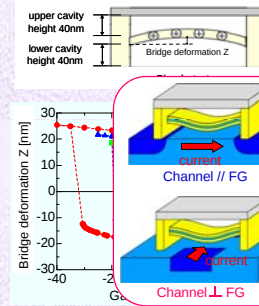
Careful structural design of the FG as well as the outer cavity needed.

Readout operation of NEMS memory



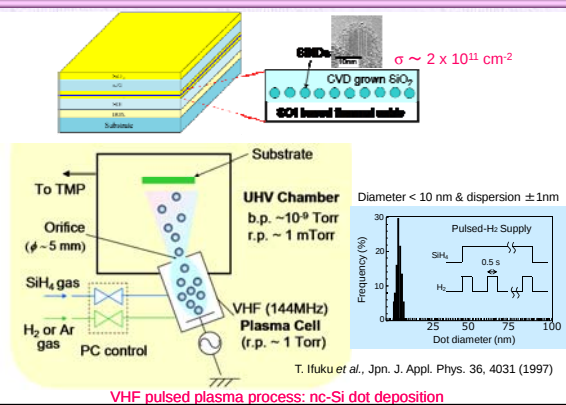
Optimized Readout characteristics

Beam & cavity structure optimization



$$P_S \propto L^{-4} T Z_0^3$$

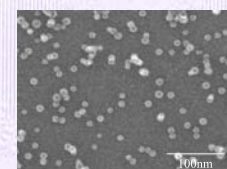
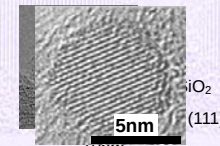
Fabrication of FG with SiNDs



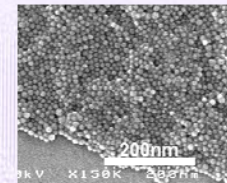
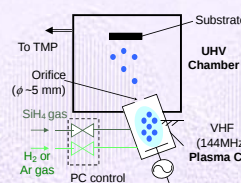
VHF pulsed plasma process: nc-Si dot deposition

Fabrication of FG with SiNDs

TEM image of a nc-Si dot

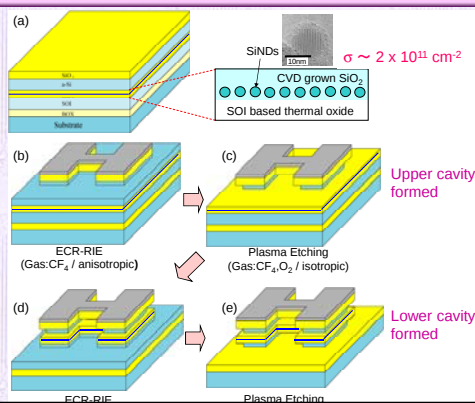


As deposited

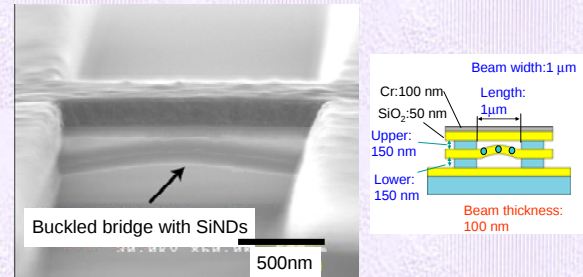


Assembled

Fabrication of FG with SiNDs

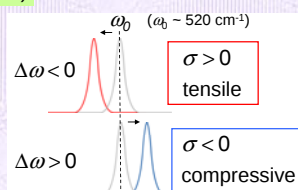
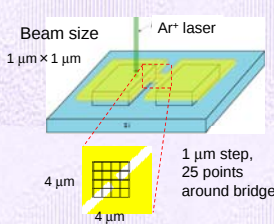


Fabrication of FG with SiNDs



Mechanical stress analysis using μRS

Micro-Raman spectroscopy (μRS)



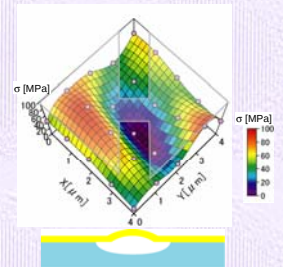
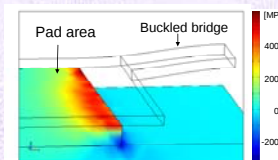
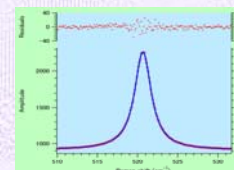
$$\sigma [\text{MPa}] = -434 \times \Delta\omega [\text{cm}^{-1}]$$

σ : Stress $\Delta\omega = \omega - \omega_b$
 ω : Raman mode frequencies of Si in presence of stress

I. De Wolf, Semicond. Sci. Technol. 11 (1996) 139-154.

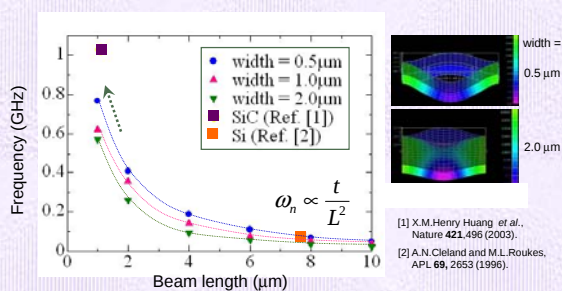
Jobin-Yvon U-1000
• 514.5 nm Ar⁺ laser source
• 1 μm spot diameter
• Resolution $\sim 0.15 \text{ cm}^{-1}$ wave number

Mechanical stress analysis using μRS



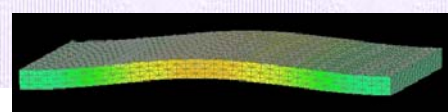
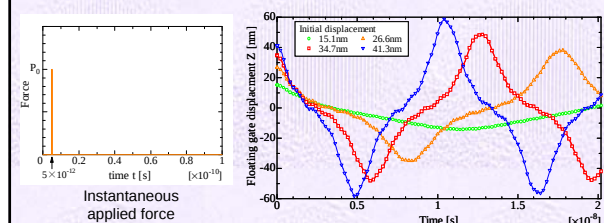
Tensile stress of about 100MPa observed around the beam edges

Switching speed of a simple flat FG



For a simple flat SiO_2 beam with $L < 1 \mu\text{m}$, over 1GHz frequency can be obtained, but.....

Switching speed of a buckled bistable FG



Oscillation at $Z_0 = 34.7 \text{ nm}$

T. Naqami et al., IEEE Trans. Electron Devices 54, 1132 (2007)

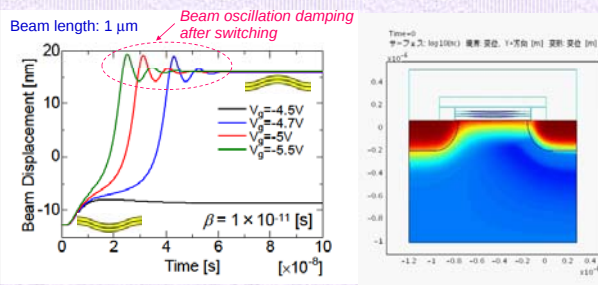
Beam damping effects on switching speed

$$m \frac{d^2 u}{dt^2} + \xi \frac{du}{dt} + ku = f(t)$$

↑ mass ↑ damping ↑ stiffness

$$\xi = \alpha_{dM} m + \beta_{dK} k$$

mass damping stiffness
 damping



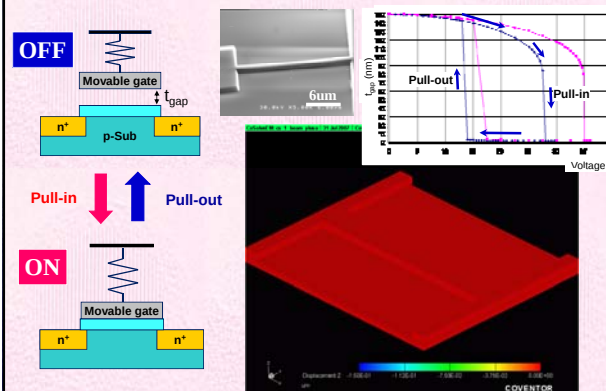
A variety of nonvolatile RAM candidates

	Cell	Flash	Nano-Crystal	FeRAM	PCRAM	MRAM	NEMS-Memory
Device Structure							
Mechanism of Non-volatility	Charge in Floating Gate	Charge in Nano-dot	Polarization	Phase Change	MR Change	Mechanical bistability	
Issues	Program Volt. reduction	Program Volt. reduction	H ₂ block CVD	Program Curt. reduction	Program Curt. reduction	Power reduction, Shock immunity	
Cell Size	4-8 F ²	4-8 F ²	10-20 F ²	8-15 F ²	8-15 F ²	6-10 F ²	
Speed	Program	10 us	10 us	<50 ns	100 ns	<50 ns	< 50 ns
	Read	<20 ns	<20 ns	100 ns	<20 ns	<50 ns	<20 ns ?
	Voltage	< 12 V	< 12 V	5 V	3 V	3 V	< 10V
P/E Cycle	10 ⁸	10 ⁸	10 ¹⁰	10 ¹²	10 ¹⁵	> 10 ¹² ?	

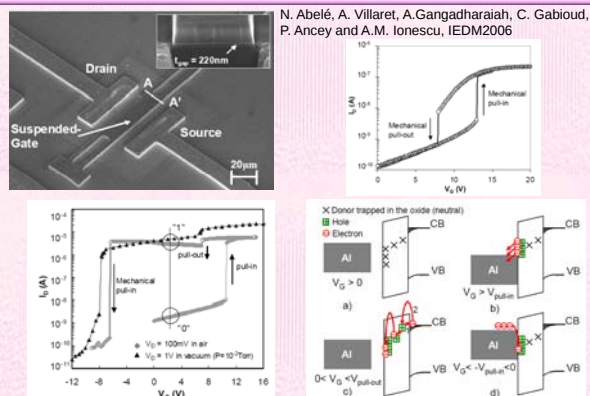
OUTLINE

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Suspended-Gate MOSFET



SG MOSFET based NEMS memory



SUMMARY

Introduction of bistable NEMS into MOS may provide a new memory device with high-speed operation & serious nonvolatility:

- **Scaling rule for a buckled FG shown**
- **Mechanical bistability demonstrated**
- **FG / cavity structure optimized for lowering programming voltage (<10V) with maintaining high ON/OFF ratio ($\sim 10^5$)**
- **Experimental FG with embedded nc-Si dots fabricated**
- **Switching speed less than 50 nsec shown for 1 μ m FG**

Acknowledgement

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