

Observation of strongly-coupled multiple-dot characteristics in the dual recess structured silicon channel with different oxidation conditions

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1. Introduction

Recently silicon single electron devices have been studied widely for various applications due to their low power consumption and multi-functionality. For ultrasensitive electrometer, single shot readout of qubit, and single electron dynamics applications radio-frequency single electron transistor (RF-SET) is the prime candidate [1,2]. The crucial requirement to realize the RF-SET applications in silicon is low tunnel junction resistance silicon SET [3]. To realize low resistance silicon SET, two extra gates can be used in the channel recesses (gates G1 and G3 in the Fig. 1) along with the island gate (G4) to tune the tunnel junction resistance.

Interestingly, single-dot and strongly-coupled multiple-dot characteristics were also observed in this structure when the oxidation time and recess dimensions were varied. Here, we report measurement results of Device A and Device B, which show single-dot and multiple-dot characteristics respectively. Multiple-dot characteristics can be attributed to the formation of a single island (shown as dotted oval in Fig.2 (b)) in each recess due to the stress induced Pattern-Dependent Oxidation (PADOX) [4].

2. Fabrication Process

SIMOX wafer with 100 nm silicon-on-insulator (SOI) and 200 nm buried-oxide layer (BOX) layer was used. Initially, substrate was oxidized and phosphorus implanted to the dose of $\sim 10^{19}$ cm⁻³. Substrate was oxidized again to reduce the thickness of SOI to 40 nm. Recess structure was patterned on the substrate using the high-resolution electron beam lithography. Electron cyclotron resonance-reactive ion etching (ECR-RIE) was done to transfer the lithographically defined pattern to SOI. After etching, thermal oxidation was done at 1000 °C to passivate surface states and to reduce the effective thickness of SOI. For Device A, lithographically defined recess length and width were 200 nm and 30 nm respectively; post lithography oxidation duration was 10 minutes. For Device B, lithographically defined recess length and width were 150nm and 30nm respectively; post lithography oxidation duration was 25 minutes (15 minutes longer than for Device A). SEM image of the fabricated recess structured SET is shown in Fig.1. The bright regions indicate SOI and the dark regions indicate the BOX layer of the substrate.

3. Results and Discussion

In this work, all the reported electrical measurements were carried out at 4.2 K and substrate was grounded. Fig. 3

shows the contour plot of the measured drain current as a function of drain voltage (V_d) and gate G4 voltage (V_{g4}) with other two gates grounded for Device A. A virtually uniform oscillation period manifests that a single charging island is responsible for the Coulomb oscillation. We assume that lateral confinement of the channel in the recess areas leads to the single island formation as shown in Fig. 2 (a). Contour plot of Device A drain current as a function of the gate voltages G1 and G3 is shown in Fig. 4 with the gate voltage G4 kept at 0 V. Observed almost parallel current peak lines assure the formation of the single charging island.

Measured coulomb oscillation characteristic of the gate G4 with gates G1 and G3 grounded is shown in Fig.5 for Device B. From this contour plot, presence of coulomb diamonds with different coulomb gaps can be noticed, which confirms the existence of extra charging islands formed in the channel. For the other two gates G1 and G3, clear coulomb oscillations were observed with different oscillation periods. Contour plot of Device B drain current as a function of the gate voltages G1 and G3 is shown in Fig. 6 with the gate voltage G4 kept at 0.04 V. In contrast to the results for Device A (Fig. 4), clear anti-crossing behaviours were observed, which indicates the extra islands are strongly coupled to the main charging islands. We attribute these characteristics observed for Device B to two extra islands naturally formed by the stress-induced oxidation inside the individual recessed regions as shown in Fig. 2 (b) as a result of narrower recess and longer oxidation time.

4. Conclusion

Formation of single and multiple dot characteristics was observed for the dual recess structured silicon channel with different oxidation conditions. We ascribe the multiple dot characteristics to the formation of an island in each recess due to the stress-induced oxidation in the narrow recess regions. As the thermal oxidation is very stable and controlled process, this recess structure can be used as a candidate of strongly-coupled Quantum Dots for solid-state quantum bits.

References

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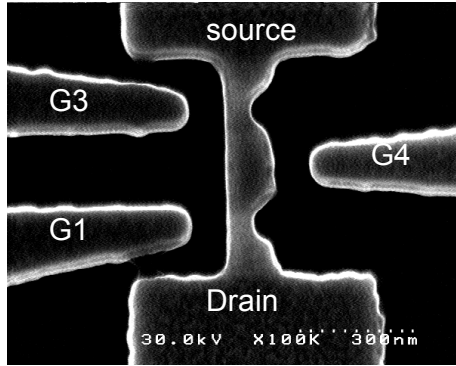


Fig.1. SEM image of the fabricated recess structured silicon channel.

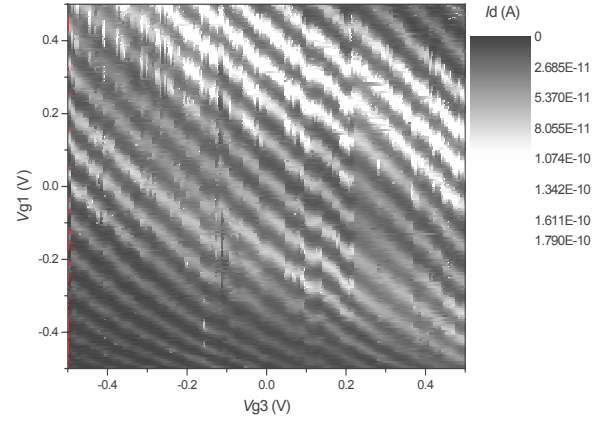


Fig. 4 Contour plot of drain current vs V_{g1} and V_{g3} at 4.2 K of Device A. $V_d=1$ mV, $V_{g4}=0$ V.

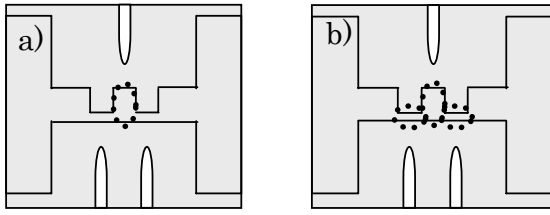


Fig. 2 Schematic diagrams of the possible location of single-dot and multi-dot (dotted oval region) in Device A (10 minutes oxidation) and Device B (25 minutes oxidation) respectively.

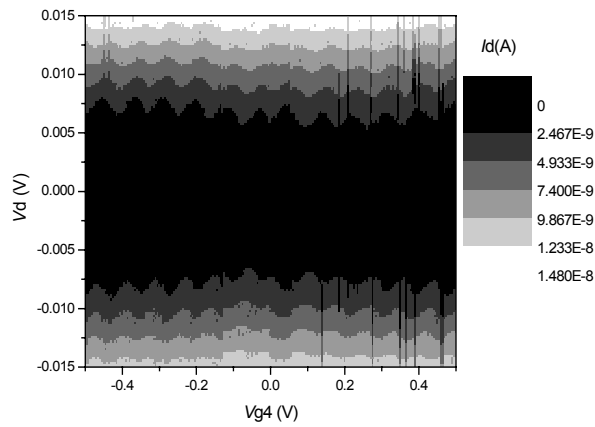


Fig. 3 Coulomb oscillation characteristics of Device A for the gate G4 at 4.2 K. Gates G1, and G3 were grounded.

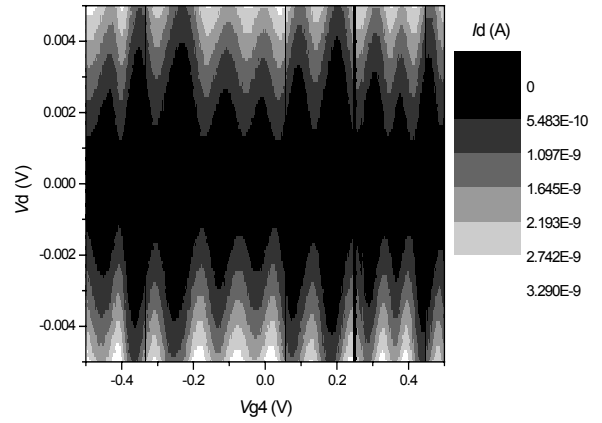


Fig. 5 Coulomb oscillation characteristics of Device B for the gate G4 at 4.2 K. Gates G1, and G3 were grounded.

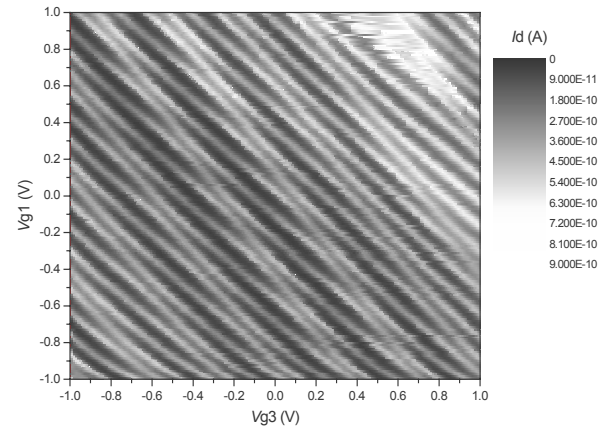


Fig. 6 Contour plot of drain current vs V_{g1} and V_{g3} at 4.2 K of Device B. $V_d=1$ mV, $V_{g4}=0.12$ V.