High-speed and Non-volatile Memory Devices Using a Macroscopic Polarized Stack Consisting of Double Floating Gates Interconnected with Engineered Tunnel Oxide Barriers

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1. Introduction

The crucial limitation of tunneling oxide thickness scaling down due to maintaining sufficient retention time, also limit the programming speed to ~ 10 μs in the conventional flash memory. While recent new high-speed non-volatile random access memories have common serious issue of developing unconventional materials, recent development of high-*k* materials fabrication technologies allow us to integrate the high-*k* oxide thin films with other advanced silicon devices. We propose a new memory device concept using novel macroscopic polarized stack which consist of double floating gates (DFGs) separated by the band-profile engineered tunnel oxide barrier. This concept is quite new and will actualize a high-speed non-volatile memory only within conventional silicon process technologies integrated with high-*k* materials fabrication.

2. Memory cell structure and operation principle

A cross sectional schematic of the device is shown in Fig. 1. The DFGs made of n^+-poly-Si are placed between the gate electrode and field-effect-transistor (FET) and are electrically isolated by block barrier SiO_2 layers. We use an $SiO_2/HfO_2/SiO_2$ (SHS) stack as a tunnel barrier between two floating gates. Tunneling current density through the SHS stack was calculated by solving the Schrödinger equation and Poisson equation in a self-consistent manner. Figure 2 shows calculated tunneling current density, J_t as a function of voltage drop at the stack, V_s. Note that the 1 nm/5 nm/1 nm SHS stack we has higher J_t-V_s slope than the single 4 nm SiO_2 has, which is consistent with the previous report [1]. We have succeeded in fabricating SHS stack structure on the SOI substrate as shown in Fig. 3.

Schematics of the operation principle are illustrated in Fig. 4.When the applied gate bias, V_g, is negative, charge in the DFGs moves through tunneling barrier and polarization upward is induced in the DFGs. This polarization was maintained after V_g was swept down to zero. In case of positive V_g application, polarization downward is induced in the same manner. These two different states of polarization in the DFGs can be sensed as the difference of source-drain current (I_{ds}) in the FET underneath. In our new memory cell, programming and erase operations are performed with charge transfer only between DFGs under an applied gate bias. The stacked DFGs structure can therefore be optimized independently of the sense MOSFET underneath. This is in contrast with the conventional Flash memory in which the program/erase operation relies on charge injection from the MOSFET into the FG via the gate oxide, and therefore the sense MOSFET and gate oxide should be optimized for both program/erase and readout operations. The stacked tunnel barrier interconnecting DFGs can be tailored to achieve extremely-high current ON/OFF ratio and to meet contradicting requirements of high-speed writing and long data retention. Furthermore, the degree of charge polarization can easily be altered by changing the structural parameters of DFGs while such adjustment is rather hard for ferroelectric materials used in 1T FRAM.

3. Characterization using SPICE simulator

We analyzed the characteristics of this memory by using the SPICE simulator. The equivalent circuit used in this analysis is shown in Fig. 5. First we estimate the programming voltage from the response to the pulsed V_g. We applied 10 MHz rectangular pulses and monitored the change of the lower floating gate voltage, V_{lfg}, which directly shows a state of polarization in the DFGs. Figure 6 shows V_{lfg}-V_g plot for different gate-pulse amplitude, V_{gm}. With increasing V_{gm}, hysteresis becomes clear and it is caused by the bistability of polarization in the DFGs. At V_{gm} = 13 V, the difference of V_{lfg} between two states, ΔV_{lfg} is about 0.5 V, which is easily distinguishable in FET sensing as shown later. Therefore we can conclude that 10 MHz operation is possible at V_{gm} = 13 V. The results suggest that the programming speed of our polarization memory is 100 times faster than that of the conventional flash memory at the same programming voltage. Figure 7 shows I_{ds}-V_g characteristics of the FET with the programming speed of 10 MHz and with V_{gm} = 13 V. The ΔV_{th} of 0.5 V between two stable states was identified. Ratio of I_{ds} at the reading voltage of 0.5 V between two states is about 10^5, which is sufficient to read the difference of two states. If we replace the block barrier layers with high-*k* materials such as La_2O_3, the V_{gm} can be reduced to 6 V as shown in Fig. 8.

4. Conclusion

We proposed the high-speed non-volatile memory concept by using bistability of polarization in the DFGs structure. 10 MHz programming speed is possible at the programming voltage of 6 V within the device fabrication which is fully compatible with the near future silicon process technology integrated high-*k* materials fabrication.

[1] B. Govoreanu *et al.*, IEEE Electron Device Lett. **24**, 99 (2003).

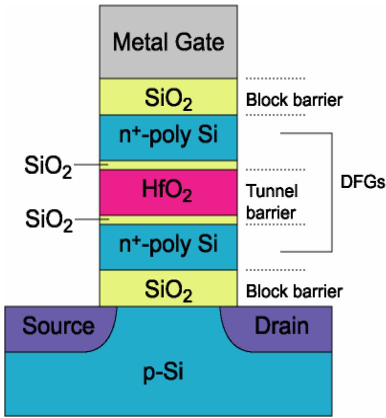


Fig. 1: A cross sectional schematic of the proposed device

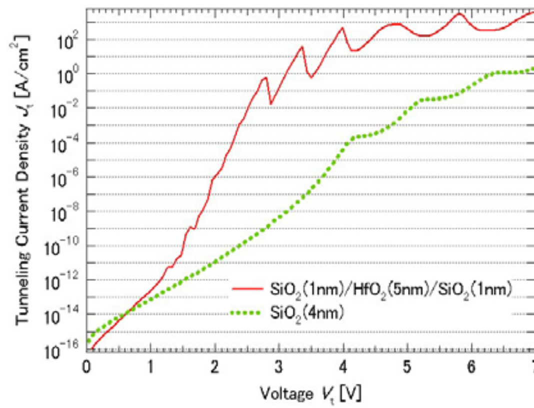


Fig. 2: Calculated J_t-V_s characteristics of SiO_2/HfO_2/SiO_2 tunnel barrier and single SiO_2 tunnel barrier

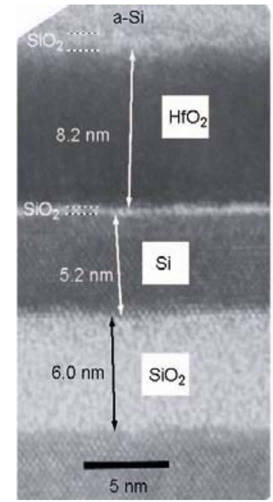


Fig. 3: Cross sectional TEM image of a part of the DFGs cell

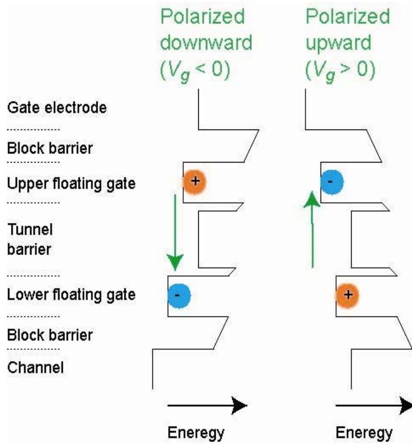


Fig. 4: Schematics of macroscopic polarization induced in the DFGs by applying gate bias

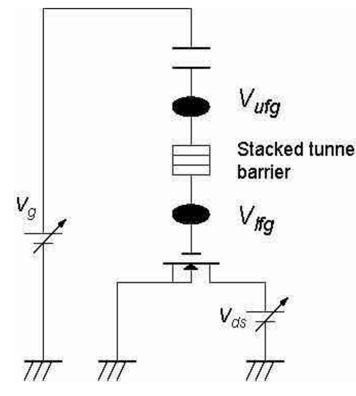


Fig. 5: Equivalent circuit models used in the SPICE simulation

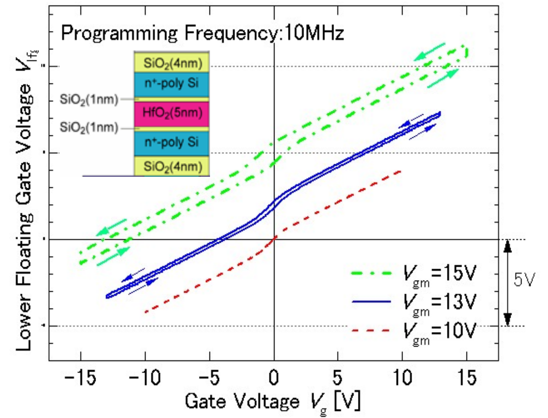


Fig. 6: Change of V_{lfg}, as a function of V_g for various V_{gm} (thicknesses of individual layers shown in the inset)

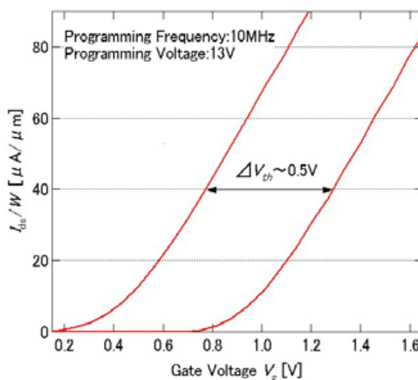
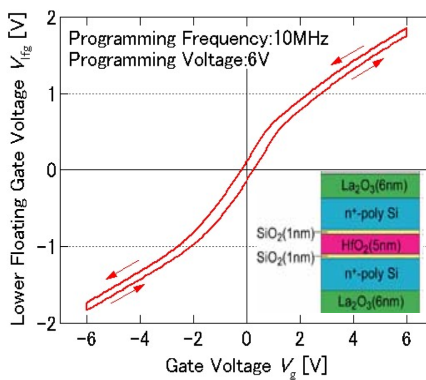


Fig. 7: I_{ds}-V_g characteristics of the FET underneath for the same stack shown in Fig. 6



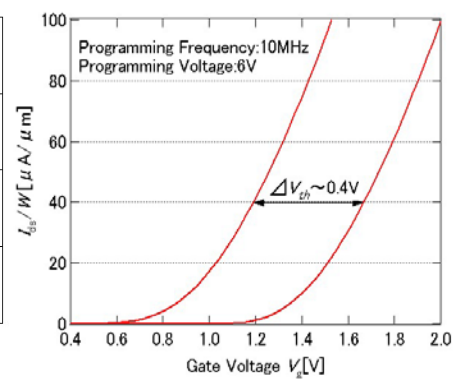


Fig. 8: In case of La_2O_3 used as block barriers (shown in the inset). (a) Change of V_{lfg}, as a function of V_g (b) I_{ds}-V_g characteristics