

# Fabrication and Characterization of Double Single-Electron Transistors as a Readout for Charge Qubits

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## 1. Introduction

Double Quantum Dots (DQDs) have been studied as a promising candidate for solid state quantum bits (qubits). Initially most of the DQD researches were done using the GaAs/AlGaAs heterostructures, where DQDs were realized through the depletion of a two-dimensional electron gas by using surface gates[1]. Recently Si-based DQDs have also been fabricated by using electron beam lithography and the reactive ion etching (RIE) technique, which is well compatible with the existing silicon fabrication process. Coherent oscillations of Si-based DQDs were also reported with long decoherence time[2]. Hereafter, it is important to study how to integrate more than two charge qubits and its readouts. As a first step to realize multiple qubit readouts, we have fabricated double single-electron transistors (DSETs) (Fig. 1), where SETs are connected in series. A pair of DQDs (double qubits) will be integrated adjacent to individual SETs by depositing nanocrystalline Si quantum dots using VHF plasma CVD technique [3]. Qubits operation will be controlled via electrodes (G1-G5). The gate electrodes G6 and G7 are used to manipulate the SET islands electrochemical potentials. To characterize this readout, we fabricated DSETs without qubits and its electrical measurements are reported in this paper.

## 2. Fabrication

DSETs without qubits were fabricated on silicon-on-insulator (SOI) substrate with multiple gates. SEM image of the fabricated DSETs without qubit are shown in Fig.1. The bright regions indicate Si ( $P$  doped  $\sim 10^{19} \text{ cm}^{-3}$ ) and the dark regions indicate the buried-oxide layer (BOX) of the SOI material. The DSETs were patterned using the high-resolution electron beam lithography in the P implanted substrate with lithographically defined diameters of approximately 90 nm for the islands. The lithographically defined pattern was transferred to SOI by using the electron cyclotron resonance-reactive ion etching (ECR-RIE) technique. At this fabrication process, thickness of the SOI layer and the BOX layer are 40 nm and 200 nm, respectively. After etching, thermal oxidation was done at 1000 °C to passivate the surface states and to reduce the effective thickness of the SOI down to 30 nm. This leads to the resulting overall dot diameter of approximately 45 nm. In this device structure, adjacent constrictions act as tunnel barriers connecting the charging islands to the source and drain electrodes. The outer constrictions are of  $\sim 30$  nm and the center constriction is  $\sim 10$  nm in width.

## 3. Results and Discussions

Electrical measurements were carried out at 4.2 K for the fabricated DSETs. Figs. 2 and 4 show the contour plots of the differential conductance ( $\partial I_S / \partial V_S$ ) as a function of  $V_{G6}$  and  $V_{G7}$  respectively, and  $V_S$ . Clear Coulomb diamonds can be observed from these plots. In case of random dopant induced SET, fluctuation of the impurities leads to unstable islands. But lateral confinement of the channel dimensions by lithography makes it possible to realize well-defined tunnel barriers. Both the differential conductance plots support it very well. Furthermore from these plots the presence of Coulomb diamonds with different Coulomb gaps is also noticed, which confirms the existence of two islands.

Source current-voltage characteristics as a function of G6 voltages from 0 V to 10 V (source current is displayed with 4 nA offset) are shown in the Fig. 3. Same kinds of characteristics were observed for G7 voltages as well. Clear Coulomb staircase characteristic was also observed from the plot for both positive and negative source voltages. In the conductance plots, outside the Coulomb blockade region lower conductance plateaus clearly indicates the Coulomb staircase characteristics. This is attributed to the high resistance of the central tunnel barrier between two islands. From the SEM image of the device it can be understood the resistance of the center tunnel barrier is larger than the other tunnel barrier resistances.

To understand further the conductance mechanism of the DSETs, equivalent circuit simulation was performed. The equivalent circuit is shown in Fig. 1 (b). For the capacitance values  $C_{G612}=0.06$  aF (G6-Island 2), and  $C_{G611}=0.02$  aF (G6-Island 1), the simulation result (Fig. 5) shows good agreement with the experimental result. Even though the device structure is symmetrical, the appearance of Coulomb staircase is noticed for the higher resistance ratio of the central tunnel barrier to the other tunnel barriers in the simulation result (Fig. 6). In addition, it was found from the simulation that the number of electrons on Island 1 and Island 2 can also be changed individually in specific gate voltage regions.

## 6. Conclusion

In this work DSETs were fabricated and the individual SET operations were analyzed by the differential conductance characteristics. Coulomb diamond with clear Coulomb staircase was observed. It was confirmed from the equivalent circuit simulation that high resistance ratio of the central barrier to the other tunnel barriers leads to Coulomb staircase characteristics.

## References

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- [2] J. Gorman et. al., *Phys. Rev. Lett.*, **95**, 090502 (2005).
- [3] Y. Kawata et al., *SSDM'06*, pp.812 (2006).

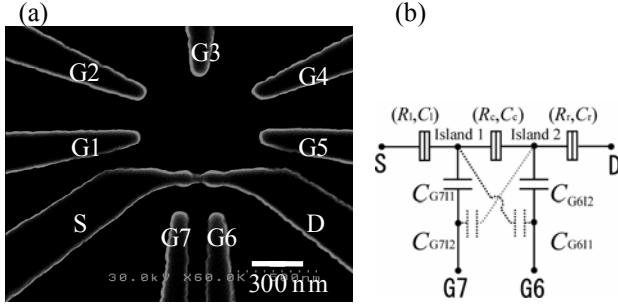


Fig. 1. (a) SEM image of DSETs with qubits gates. (b) The equivalent circuit of the DSETs.

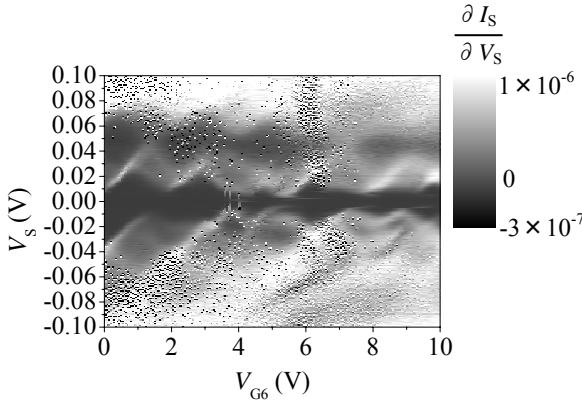


Fig. 2. Contour plot of the measured differential conductance  $(\partial I_S / \partial V_S)$  as a function of  $V_{G6}$  and  $V_S$  at 4.2 K.

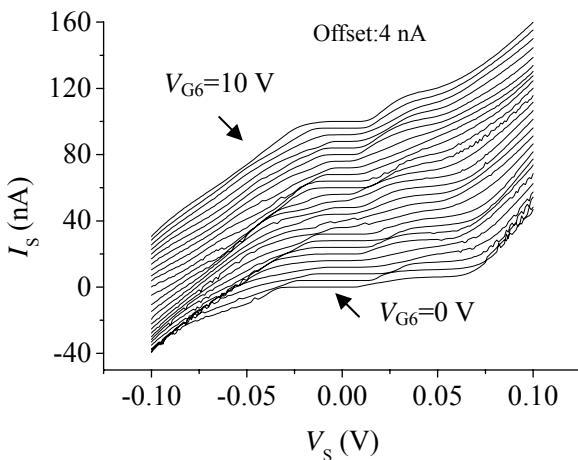


Fig. 3.  $I_S$ - $V_S$  characteristics as a function of  $V_{G6}$  from 0 V to 10 V at 4.2K (displayed with 4 nA offset).

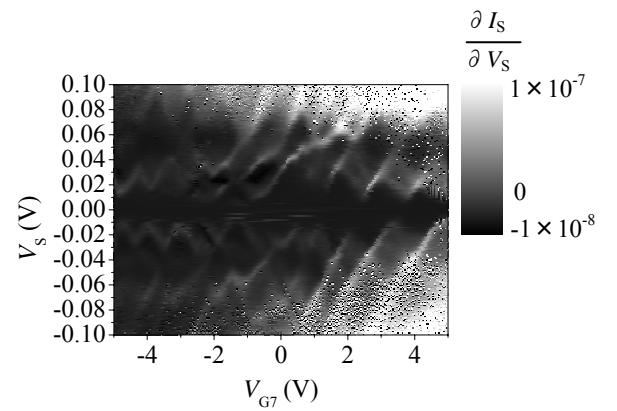


Fig. 4. Contour plot of the measured differential conductance  $(\partial I_S / \partial V_S)$  as a function of  $V_{G7}$  and  $V_S$  at 4.2 K.

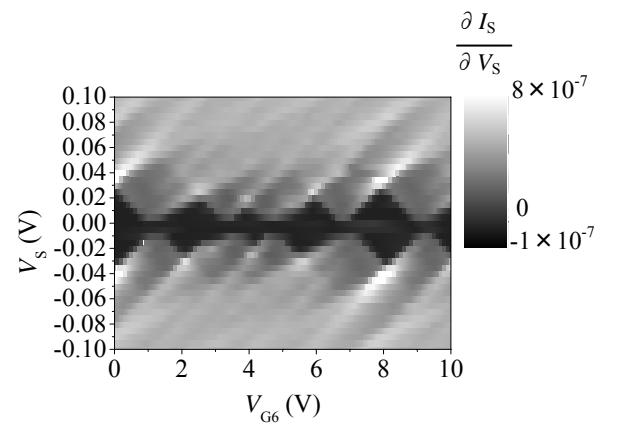


Fig. 5. Contour plot of the simulated differential conductance  $(\partial I_S / \partial V_S)$  as a function of  $V_{G6}$  and  $V_S$ .

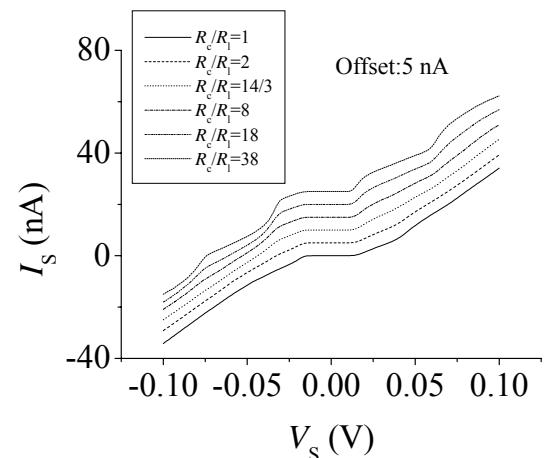


Fig.6.  $I_S$ - $V_S$  characteristics at various ratios of central tunnel barrier resistance  $R_c$  to the other tunnel resistances  $R_l$  and  $R_r$  ( $R_l = R_r$ ) at  $V_{G6} = 1.8$  V (displayed with 5 nA offset).