Voltage-limitation-free compact SET model incorporating the effects of spin-degenerate discrete energy states

Benjamin Pruvost[1], Hiroshi Mizuta[1,2], and Shunri Oda[1,2]
[1] QNERC & Dept. of Physical Electronics, Tokyo Institute of Technology
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, JAPAN
and [2]SORST JST (Japan Science and Technology)
E-mail: benjamin@neo.pe.titech.ac.jp, Phone: +81-3-5734-2542, Fax: +81-3-5734-2542

1. Introduction

Among all post-CMOS VLSI candidates, single-electron transistors (SETs) have attracted much attention due to their ultra-low power consumption and highly functional features. As well as logic-circuit applications [1], new hybrid devices combining SETs with MOSFET and/or nano electromechanical systems (NEMS) have been recently investigated [2],[3]. However, simulation of hybrid circuits featuring SETs in a SPICE-like environment is fairly difficult because of the electrical characteristics of SET that result from the Coulomb blockade phenomenon and accurate but time-consuming Monte Carlo simulations [4],[5] are not adapted to design realistic circuits featuring a large number of components. Therefore, accurate SET analytical models are required to allow fast co-simulations with MOSFETs and NEMS models.

Until now, several physically based analytical models have been reported, but they all have a working voltage limitation [6],[8]. As mentioned in [8], although the Coulomb blockade only occurs for drain to source voltage $|V_{DS}|$ lower than e/C_Σ (where C_Σ is the total island capacitance with respect to the ground), models valid for V_{DS} higher than e/C_Σ are needed once the SET is biased by a current source or a MOSFET. In this work, we propose a physically based compact analytical SET model, derived on the basis of the "orthodox" theory of single charge tunneling and the master equation method, which virtually shows no voltage limitation in the scope of this theory. We also show how the discreteness of the quantum energy levels in the case of a silicon-based SET operating at room temperature modifies the approach and discuss the observed quantum mechanical effects.

2. Voltage-limitation-free compact SET model

The idea is to consider only the states that are essential, depending on the values of V_{DS} and to make the model able to adapt its complexity to the operating voltage by itself. Thus, the accuracy remains excellent whatever the bias and the calculation time is always kept to the shortest possible. The model is verified against Monte Carlo simulation [5] with excellent agreement. It describes accurately SET characteristics for a wide range of temperatures ($T < e^2/(10k_BC_\Sigma)$), can take the background charge effect into account and is valid for single-gate as well as multi-gate devices. It is then compared to reported models. Whereas usual extensions uselessly make the model more complex hence more time-consuming at low bias and, be that as it may, are inescapably limited, our model self-adapts its complexity so that it remains accurate and as fast as possible whatever the operating voltage or the current bias applied to the SET.

3. Effects of spin-degenerate discrete energy states

The operation of SET at room temperature requires an extremely small feature size. However, for these dimensions, the quantum confinement energy cannot be neglected compared to the other energies (charging and thermal energies). This means that the energy levels in the dot are quantized and the quantum level spacing will determine the transport characteristics: one gets off the scope of the orthodox theory. We discuss a way to take the discreteness of the quantum energy levels into account by solving the master equation for a given number of states. To the best of our knowledge, only one analytical model taking into account the quantum-level spacing has been reported until now [9]. However, this model does not consider the levels spin-degeneracy, and propose a different approach concerning the links between the states. This approach enables us to introduce in the model experimentally observed quantum effects such as negative differential conductance (NDC).

4. Summary

A physically based compact SET model which virtually shows no limitation in the scope of the orthodox theory has been reported and verified against Monte Carlo simulator with excellent agreement. It is valid and accurate whatever the drain voltage or the current bias and faster than reported models on the whole. A way to integrate in the model the effects of spin-degenerate quantum energy levels discreteness in the case of a silicon-based SET was also introduced and observed quantum mechanical effects, such as negative differential conductance (NDC), were discussed.

References

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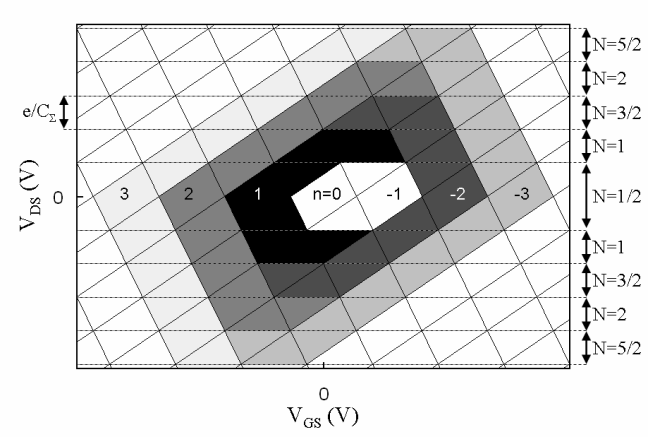

Fig. 1 Representation of the (V_{DS},V_{GS}) space paving in our model: the number of states taking into account increases by one with each V_{DS} step of e/C_Σ.

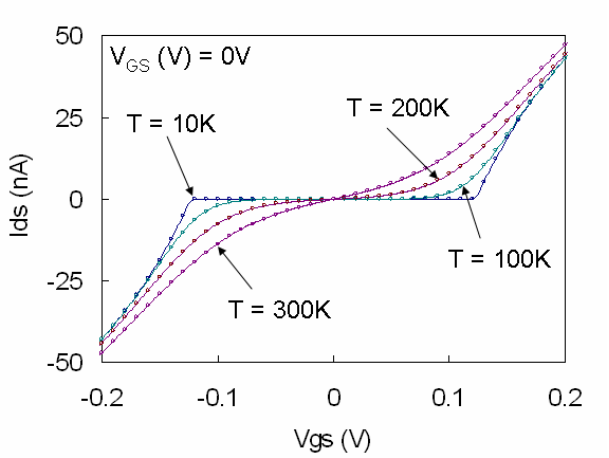

Fig. 2 I_{DS}-V_{GS} characteristics of our model at different temperature levels for symmetric device with C_G=0.2aF, C_D=C_S=0.15aF and R_D=R_S=1MΩ, at T=173K. Here dotted line represents Monte Carlo simulation [5] and solid line represents our model.

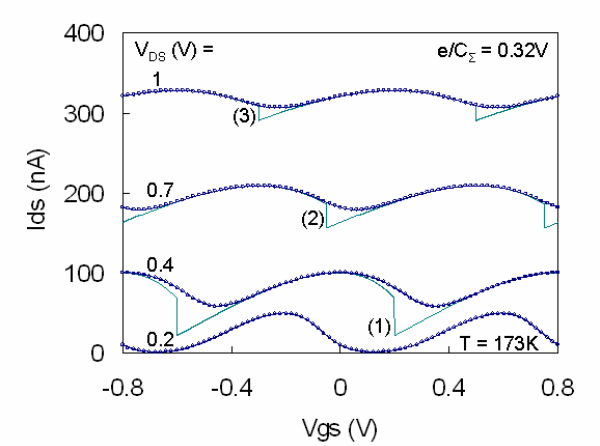

Fig.3 Comparison of our model (unbroken solid line) with different reported-like models (broken solid line):
(1) | V_{DS} |< e/C_Σ-limited model [6],
(2) | V_{DS} |< $2e/C_\Sigma$-limited model [7],
(3) | V_{DS} |< $3e/C_\Sigma$-limited model [8].
Dotted line represents Monte Carlo simulation [5]. Here device parameters are C_G=0.2aF, C_D=C_S=0.15aF and R_D=R_S=1MΩ, at T=173K.

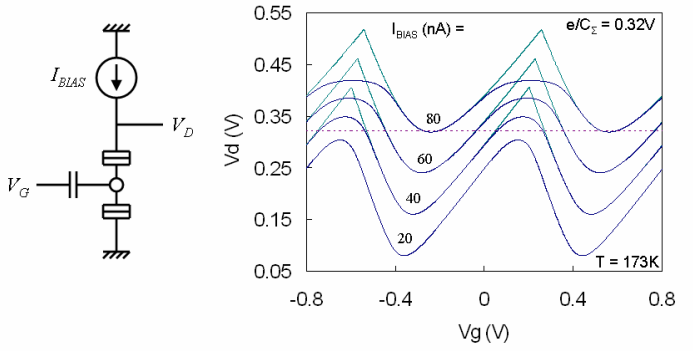

Fig. 4 Comparison of our model (unbroken solid line) with a | V_{DS} |< e/C_Σ-limited mode (broken solid line) for a current biased SET. Here device parameters are C_G=0.2aF, C_D=C_S=0.15aF and R_D=R_S=1MΩ, at T=173K.

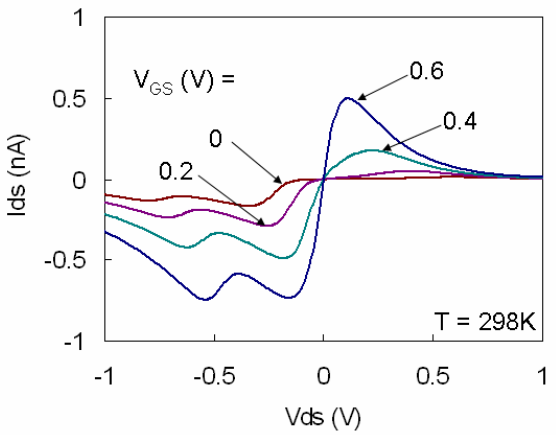

Fig. 5 Simulated I_{DS}-V_{DS} characteristics of a silicon-based SET having a 5nm large island operating at T=298K. The NDC is clearly visible for negative bias.

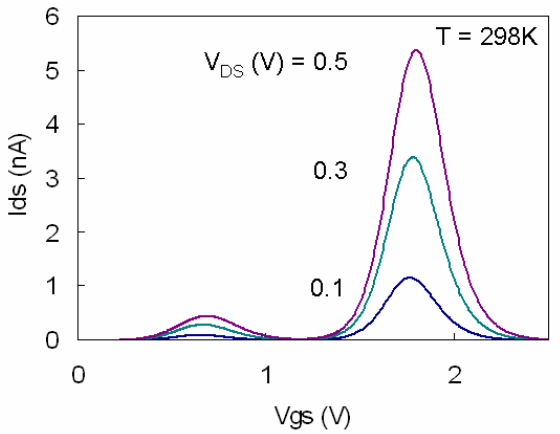

Fig. 6 Simulated I_{DS}-V_{GS} characteristics of a silicon-based SET having a 5nm large island operating at T=298K. Coulomb oscillations do not have the same amplitude.