Top-down and bottom-up approaches towards silicon nanoelectronics

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1. Introduction

The performance of silicon-based VLSI circuits has steadily been improved by scaling down device dimensions, and a nearly exponential growth of microelectronics capabilities has been achieved. However, maintaining this top-down miniaturization trend is getting exceedingly hard due to fundamental physical and technological limitations as well as of the economical limitation. Nonconventional bottom-up approach has attracted much attention along with recent progress of techniques for fabricating size-controlled silicon nanodots (SiNDs) and nanowires (SiNWs). Individual SiNDs and SiNWs maintain superior electron transport properties, and high-performance nanoelectronic devices may be fabricated by integrating these Si nanostructures as a building block. In addition, the Si-based bottom-up approach may lead to high- performance and large-area electronics as the SiNDs and SiNWs can be assembled both on Si and non-Si substrates such as glass and plastic. Moreover, zero- and one-dimensional nature of electronic states in the individual SiNDs and SiNWs realizes new electronic and photonic properties which are not achieved with bulk silicon. Combining the bottom-up approach with the conventional top-down Si technologies enables us to explore silicon nano-, micro- and macro-electronics on the common technical footing.

This paper presents a brief review of our recent work investigating a novel bottom-up approach to realize silicon based nanoelectronics. We discuss fabrication technique, electronic properties and device applications of silicon nanodots as a building block for nanoscale silicon devices.

2. Combining bottom-up and top-down approaches for fabricating nanoscale device structures

Integrating the fabricated SiNDs, either over a large area or in a local area, is a very challenging issue. Various techniques are currently under investigation, for example, the dispersion solution drop & evaporation method, the Langmuir Blodgett (LB) method and the nano template method. We also examined a novel method of fabricating nanoscale devices by conducting the self-assembly of the SiNDs on patterned nano electrodes. For preparing the dispersion solution, SiNDs deposited on the were soaked into the solvents such as methanol or isopropanol, and the ultra sonic treatment was applied for a few tens seconds. The SiND solution was then condensed by evaporating the solvent a fraction.

The nanoelectrodes were fabricated by using the electron beam lithography on the heavily-doped n-type silicon on insulator (SOI) substrate. This structure gives a good areal contrast of hydrophobic (Si) and hydrophilic (SiO_2) surfaces and works as a template for the following SiND assembly process. We used a drop and evaporation technique to assemble the SiNDs from the dispersion solution by using the lateral capillary meniscus force. Figure 1 shows the SiNDs assembled on the SOI substrate with a patterned nanogap of about 35 nm. We observed that SiNDs remained only in the SiO_2 regions and were assembled near the nano gap, resulting in a SiND channel between the electrodes. This trend was observed in common over the large area. This method may be useful to fabricate the SiND based nanoscale transistors, and we believe that it is possible to form a channel with few SiNDs or even a single dot by reducing the density of SiNDs and optimizing evaporation conditions.

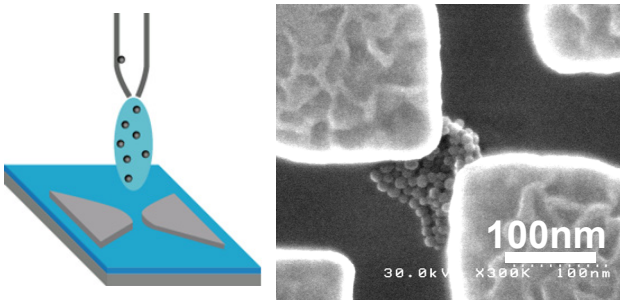

Fig. 1 SiNDs integrated onto nanoelectrodes

3. Novel functional SiND device applications

(1) Ballistic electron emission device

As one of the promising applications of the SiNDs we investigated the SiND based electron surface emitter. Unique phonon properties of the array of SiNDs covered with SiO_2 lead to ballistic electron emission phenomenon. An electron emitter device was fabricated by using a 150-nm-thick layer of SiNDs deposited on n^+-Si substrate and a very thin Au top electrode (Fig. 2). When the voltage is applied across the SiND layer, only electrons with energy higher than the Au work function W_{Au} of approximately 5 eV are emitted into vacuum through the top electrode. Both diode and emission currents were measured as a function of the extraction voltage V_{ex}, and the emission efficiency can be as large as 5%.

We also investigated the energy distribution of emitted electron by using a conventional ac-retarding-field analyzer. We found that the energy distribution of the

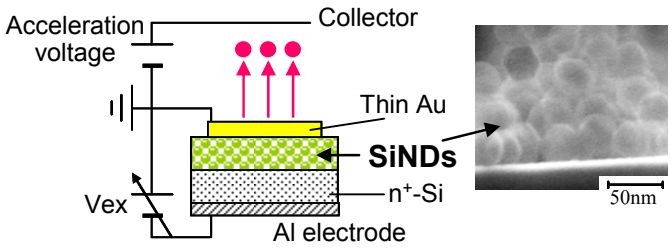

Fig. 2 Ballistic electron emitter based on stacked SiNDs

emitted electrons is non-Maxwellian in contrast with those observed for conventional cold emitters. Maximum electron energy agrees approximately with $eV_{ex} - W_{Au}$, and the peak energy varies in proportion to V_{ex}. These results show that fractional electrons travel throughout the SiND layer in a quasi-ballistic manner and emit into vacuum.

(2) Nanoelectromechanical memory device

A new nonvolatile memory concept has recently been proposed, based on the bistable operation of the sub-μm-long NEMS structure, combined with the SiNDs (Fig. 3; above). It features a suspended SiO_2 beam which incorporates the SiNDs as single-electron storage (Fig. 3; below). The beam may be moved via the gate electric field, and its positional displacement is sensed via a change in the drain current of the MOSFET underneath.

A free-standing SiO_2 single beam was first fabricated using a Si undercut etching technique. Most fabricated samples show the beams bent upwards as a result of mechanical stress, stored in the SiO_2 being released. The mechanical bistability of the beam was demonstrated by using the nano-indentor type loading system. Also, a top gate electrode has been fabricated successfully above the SiO_2.

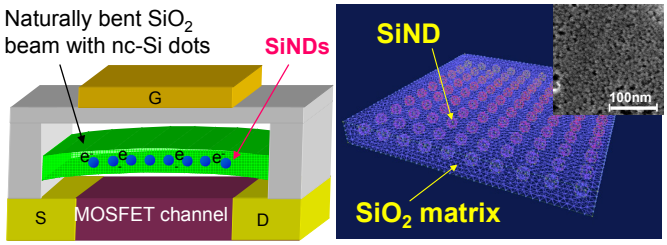

Fig.3 NEMS memory (left) and a floating gate incorporating SiND array (right)

The switching speed and power of the beam have been studied intensively by using a 3D FEM simulation. The switching speed increases approximately in inverse proportion to the beam length L and goes beyond 1 GHz in the sub-μm regime. The switching voltage of less than 10 V has recently been demonstrated for an optimized beam structure along with the scaling properties of the beam. In contrast with other emerging nonvolatile memories such as MRAM or PCRAM, the NEMS memory can still be manufactured within the conventional Si technologies.

(3) Nano information devices

Charge quantization and Coulomb blockade have also been studied intensively for SiNDs. Coulomb oscillation of tunneling current has been observed at room temperature by using point-contact single electron transistors (PC-SETs) with very few SiNDs in the channel. Electrostatic and coherent coupling effects have also been studied recently for strongly-coupled double SiNDs by using PC-SETs fabricated on a nc-Si thin film. The PC-SETs with a very small channel with 30 nm × 30 nm in lateral dimensions were formed on a 40 nm thick nc-Si film with lateral grain size of 20 – 25 nm. The electrostatic potential on the grains are controlled via the bias applied to two side gates.

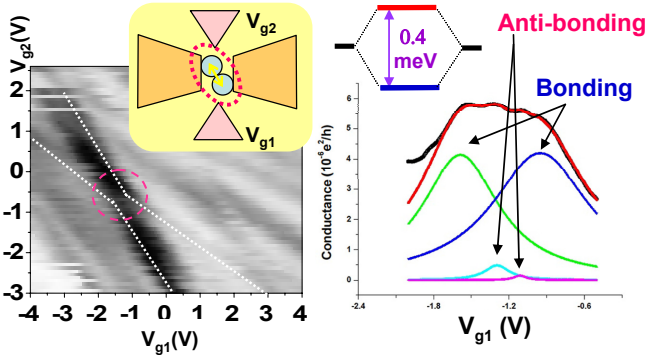

Fig. 4 Coherent electron coupling observed for strongly-coupled double SiNDs

In Fig.4, the peak lines in this plot (white dotted lines) show strong splitting (a dotted circle) caused by electrostatic interactions when the energy levels in the two dots are in resonance. In the strong coupling region, we observed that the characteristics are decomposed into four Lorentzian peaks – two main peaks with two small peaks (Fig. 4; right figure). This is attributed to the tunnel coupling across two adjacent double dots, resulting in bonding- and anti-bonding-like resonance peaks. Tunnel splitting obtained from the peak separation is about 0.4 meV, which is from a few time to an order-of-magnitude larger than the value reported previously in GaAs/AlGaAs quantum dots. Such quasi-molecular states may be used to realize a Si-based charge qubit.

4. Conclusion

We have studied SiNDs as a promising building block for Si nanoelectronics. An innovative fusion of top-down and bottom-up silicon technologies may lead to a high-performance & low-cost material platform for macro-, micro- and nanoelectronics.

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