SILICON NANOELECTROMECHANICAL INFORMATION DEVICES – PRESENT AND FUTURE –

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Present trend – From MEMS to NEMS –

Over the past few decades, the performance of VLSI circuits has steadily been improved by scaling down CMOS device dimensions. The ITRS 2005 shows that the 'Nano Era' for the CMOS devices has started in 1999 with the gate length being shorter than 100 nm (see Fig. 1) The roadmap also predicts that this miniaturization trend will be pursued further, and the gate length will reach below 10 nm in 2016. Along with such an aggressive miniaturization trend of the Si VLSI devices, various microelectromechanical devices have recently been developed by making the characteristic length (such as the resonator length) shorter in an attempt to increase their operation frequency. For example, the oscillation frequency of over 1 GHz has been demonstrated for the 1.1-μm-long SiC based beam. Dimensions of the MEMS structures reported recently are also shown in Fig. 1: the MEMS technology has just reached 1 μm regime and is now proceeding to the submicron regime. If we adopt the same definition of 'Nano Era' as that for CMOS, the present trend indicates that the nanoelectromechanical systems (NEMS) era would come between 2010 and 2015. In this paper we will discuss the physics and applications of silicon based NEMS information devices.

Fast & nonvolatile Si NEMS memory

A new nonvolatile memory concept has recently been proposed based on bistable operation of the sub-μm-long NEMS structure combined with the nc-Si quantum dots (Fig. 2). It features a suspended SiO_2 beam, which incorporates the nanocrystalline (nc-) Si dots as single-electron storage. The beam may be moved via the gate electric field, and its positional displacement is sensed via a change in the drain current of the MOSFET underneath. A free-standing SiO_2 single beam has first been fabricated using a Si undercut etching technique (Fig. 3). Most fabricated samples showed upward-bent beams as a result of release of mechanical stress stored in SiO_2. The mechanical bistability of the beam was demonstrated by using the nano-indentor type loading system. A SiO_2 beam with a top gate electrode has also been fabricated successfully (Fig. 4). The switching speed and power of the beam have been studied intensively by using a 3D FEM simulation. The switching speed increases approximately in inverse proportion to the beam length L and goes beyond 1 GHz in the sub-μm regime (Fig. 5). The switching voltage of 15 V has recently been demonstrated for an optimized beam structure along with the scaling properties of the beam (Fig. 6). In contrast with other emerging nonvolatile memories such as MRAM or PCRAM, the NEMS memory can still be manufactured within the conventional Si technologies. In addition, by further optimization, it may exhibit excellent characteristics comparable to them.

New nanoelectromechanical & phononic phenomena in Si hybrid NEMS-MOS-SET structures

Downscaling the structures into deep sub-μm and further into sub-100-nm regime, we may explore new properties of Si NEMS structures. For example, we expect phonons and electron-phonon interaction in a nanoscale bridge structure which is acoustically isolated from the Si substrate (Fig. 7) show different properties from those in bulk Si. In addition, by combining the nanobridge (1D) structures with nc-Si dot (0D) structures, new electromechanical phenomena may emerge, such as phononic bandgap & phonon confinement (Fig. 8), reduction of electron-phonon interaction, phonon blockade, metal-insulator transition, quantization of nanomechanical motion, and strong coupling of nanomechanical and electron motions. These may lead to novel functional Si nano information devices which are not achieved by using the conventional bulk Si CMOS technologies.

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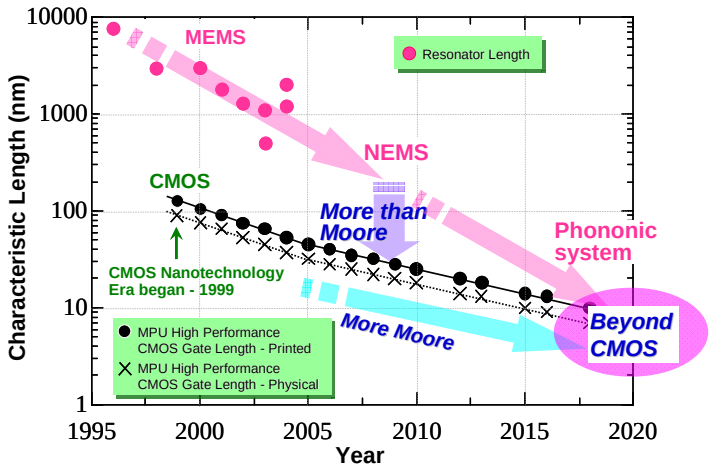

Fig.1 Trend of CMOS gate length downscaling (taken from ITRS 2005) and that of recently-reported MEMS resonators.

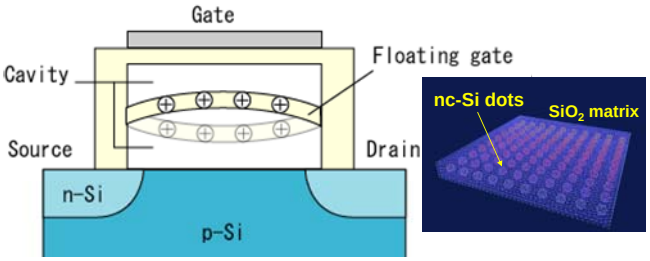

Fig.2 Schematic cross sectional view of nonvolatile NEMS memory and its beam structure.

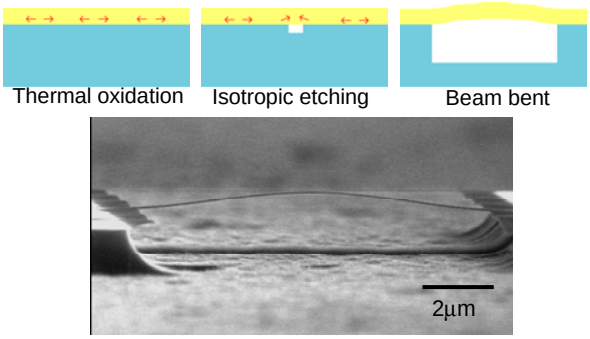

Fig.3 Fabrication method and a SEM image of a fabricated single beam naturally bent upward.

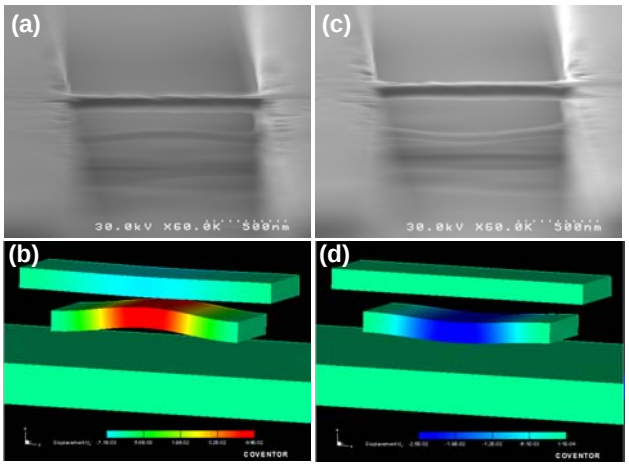

Fig.4 Fabricated and simulated NEMS beams with a top gate electrode at its bistable states.

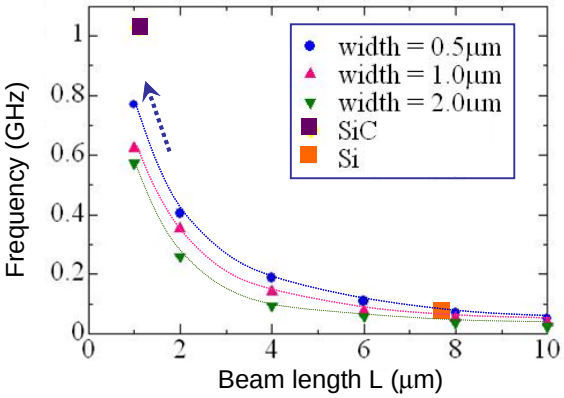

Fig.5 Calculated beam length dependence of the beam switching frequency.

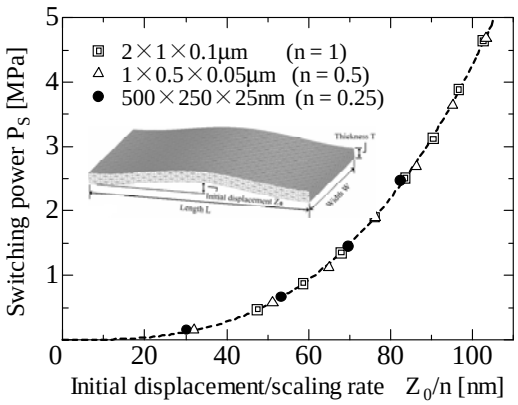

Fig.6 Calculated initial beam displacement dependence of the switching power.

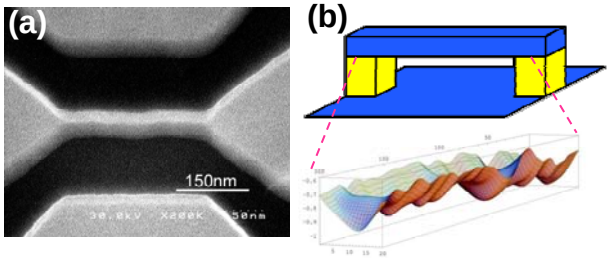

Fig.7 NEMS transistor with a heavily doped Si bridge (a) and potential landscape in the bridge (b).

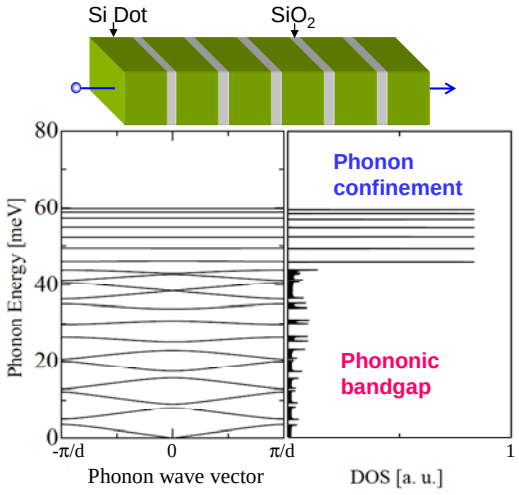

Fig.8 Si/SiO2 acoustic superlattice wire and its phononic bandgap property.