Fabrication of vertical nanopillar devices

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Key words: (Silicon, Nanopillars, Electron emission, Electroluminescence, photoluminescence)

Electron transport in silicon nanopillars has been investigated, with a view to fabricate vertical electron emission, electroluminescent and photoluminescent devices. Figure 1 shows schematic diagram of the device. Arrays of nanopillars were fabricated in highly doped single crystal silicon and polysilcon materials. A natural lithography technique utilizing colloidal gold particles as an etch mask [1], in conjunction with standard microfabriction techniques, was used to fabricate the nanopillars in selected regions. The nanopillars height was 100 nm in single crystal silicon material and 40 nm in polysilicon material and the diameter of these nanopillars was 30 nm in both cases. Figure 2 (a) and (b) shows deposited colloidal particles and nanopillars after reactive ion etching respectively. The electrical isolation of the pillars and surface planarisation was achieved by spin coating and curing a polyamide film and then etching back in oxygen plasma to expose the pillar tops. Figure 2 (c) shows the pillars coming out of polyamide film. A top contact was supported on polyimide film.

The electrical measurements presented here are from devices measured using a cryogenic temperature prober BCT-43MDC from Nagase & Co. Ltd. with a base temperature of about 20 K, and an Agilent 4156A parameter analyser. An example of the current versus voltage (*I-V*) characteristic of a nanopillar array with 30 nm diameters and 100 nm high pillars is shown in figure 3. This device consists of ~ 16 μm^2 area. Within this area ~ 600 of nanopillars are present, estimated from the packing density. The pillars are in contact with silicon below and with the top-metal contact above. The polyamide planarised layer containing the pillars acts as an insulator, in which the pillars are embedded. The I-V characteristics show only a small current ~ nA at low bias less than ~ |1.5| volts. This suggests that a large bias to conduction exits in the pillars. Because of the surface depletion effects in our nanopillars, the pillars are likely to behave as semi-insulating semiconductor. The Au-pillar interface may also form a Schottky junction. A high electric field is formed across the isolating layer, when a bias voltage is applied to the diode. Under the positively biased condition, electron are thermally injected from the *n*-type substrate into the wires and drifted towards the metal electrode by the electric field. A similar kind of operation mechanism has been suggested for electro luminescent devices based on silicon nanopillars [2, 3] and ballistic electron emitting porous silicon diode [4].
By reducing the thickness of the top Au contact to 10-15 nm these devices may be converted to electron emission, electroluminescent or photoluminescent devices, similar to that suggested by Nishiguchi et al. [5]. Future work, therefore, will investigate electron emission, electroluminescence and photoluminescence from vertical nanopillar devices with thin top contact ~ 10 nm thick. Packing density of these devices can be increased by increasing the colloidal particles deposition time and hence efficiency of these devices can be increased [2].

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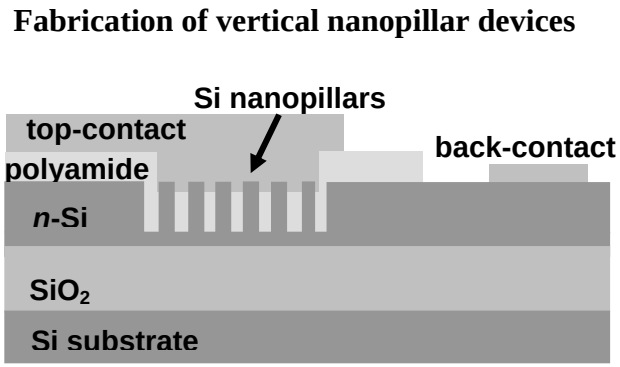

Figure 1 Schematic diagram of the a Si nanopillar device

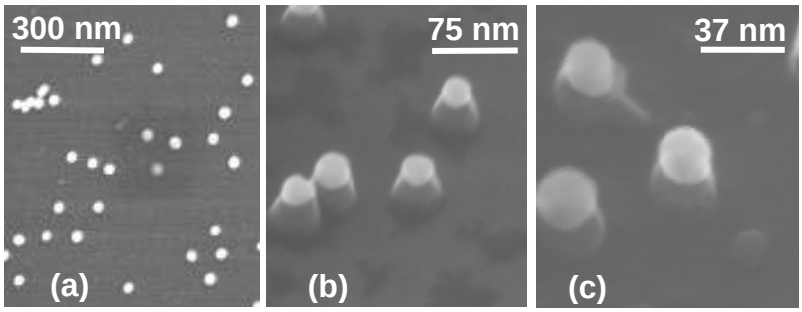

Figure 2 scanning electron micrograph of (a) 30 nm gold colloidal particles deposited on *n*-Si (b) nanopillars after etching with colloidal particles on top (c) nanopillars coming out of polyamide film after etching in oxygen plasma

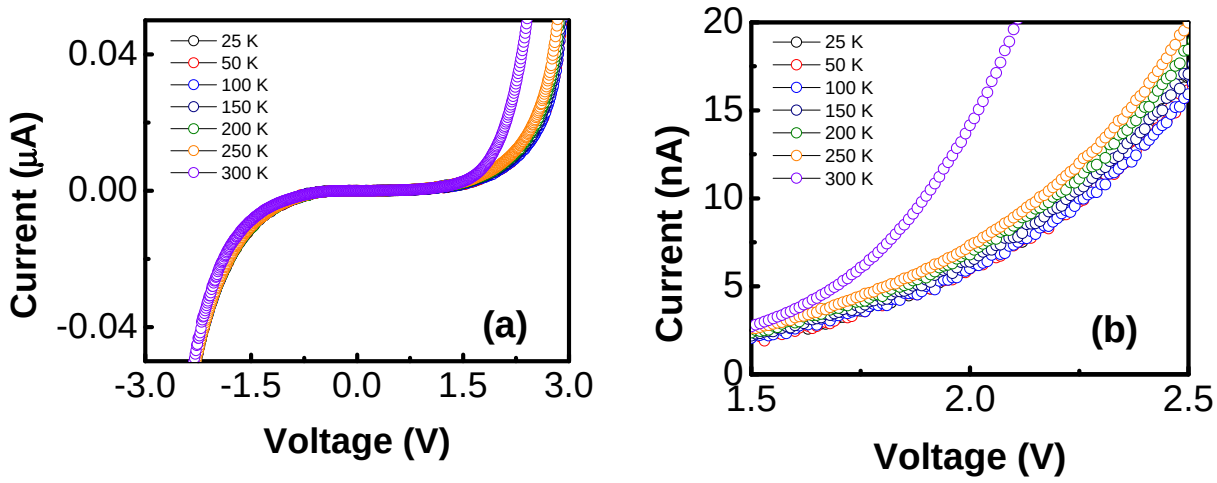

Figure 3 *I-V* characteristics of a vertical Si nanopillar device with an area of 16 μm ^{2} from 25 – 300 K (a) for both negative and positive biases (b) zoomed on positive side to show the temperature dependence