Design and Analysis of Functional NEMS-gate MOSFETs and SETs

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1. Introduction

Hybrid circuits featuring SET, CMOS and MEMS/NEMS devices are getting increasing interest as very attractive candidates for future low power and multi-functional nano-scale ICs. Introduction of nano electromechanical structures into conventional MOSFETs and SETs may provide superb performance and numerous new functionalities that are not achieved using present devices. In this way, a combination of MEMS and solid-state MOS transistor, which could act as a current switch or as a tunable capacitor, was investigated based on numerical simulation and analytical modeling [1]-[2], and a very recent report experimentally demonstrated its virtues [3]. Another recent report also proposed a design combining a nano-scale movable gate and a transistor, which could lower the threshold voltage and enhance the drive current [4]. Similarly, it has also been suggested that variable NEMS capacitor could add new functionalities to conventional SETs such as tunable capacitance [5]. Therefore, the design of the movable gate is essential to achieve the performance predicted by the numerical simulation. However, it cannot be investigated in an efficient manner if not modeled in a 3-D context. In this work, we present different designs of movable electrodes and report expected results based on 3-D calculation and analytical modeling for both MOS-NEMS and SET-NEMS architectures.

2. SET Analytical model

Simulation of hybrid circuits in a SPICE environment is fairly difficult because of the electrical characteristics of SET that result from the Coulomb blockade phenomenon. Accurate but time-consuming hybrid simulator [6] is not adapted to design realistic circuits featuring a large number of components. Therefore, accurate SET analytical models are required to allow faster simulations. We proposed a physically based compact SET analytical model for hybrid simulation. The model describes SET characteristics accurately for a wide range of drain to source voltages ($|V_{DS}| < 4e/C_{\Sigma}$) (Fig.1) and temperatures ($T < e^2/(10k_B C_{\Sigma})$) (Fig.2). It can also take the offset charges effect into account. We implemented this model in the SmartSpice circuit simulator [8] and we successfully simulated several SET circuits and hybrid circuits that have been experimentally demonstrated.

3. NEMS-gate architecture simulation

Combining the 3-D calculation and analytical modeling, we performed several simulations of hybrid devices, including MOS-NEMS and SET-NEMS structures. The movement of the metal gate is simulated by using the COMSOL simulator [7], which enables to design realistic 3-D device structures (Fig.3 and Fig.5), and results are compared to theoretical numerical simulation. A tunable capacitor model is then embedded in the SmartSpice circuit simulator [8] and coupled either with a transistor model for MOS-NEMS or with our SET analytical model for SET-NEMS.

In this work, we studied the suspended-gate MOSFET (Fig.3), which combines a solid-state MOS transistor and a suspended metal membrane in a metal-over-gate architecture [1]. One of the unique characteristics of this device is its super-exponential dependence of Q_{inv} vs. V_g in the sub-threshold region (Fig.4), which can break theoretical limits of the solid-state MOSFET such as its sub-threshold slope ideal limit of 60mV/decade, resulting of the ultra-abrupt movement of the metal membrane.

We also investigated SET-NEMS devices (Fig.5) in term of the modulation of Coulomb oscillations. By tuning the gate capacitance of the SET, one can change the total island capacitance and hence control the periodicity of the current (Fig.6). Such periodicity encoding of the current could be used in communication system to get rid of the unwanted background charge effect. NEMS gate architectures could also enrich conventional SETs with new functionalities such as threshold gate behavior or abrupt current switching, and in a general manner, further control of the device's behavior.

4. Summary

We have studied both NEMS-gate MOSFET and NEMS structures by combining 3-D design and a newly-developed SET analytical model. Our hybrid simulation has enabled us to investigate new functionalities that could be added to conventional MOSFET and SET such as very abrupt current switching, memory, or further control of the device's behavior.

References

[1] A. Ionescu *et al.*, *Proc. of ISQED 2002*, pp.496-501.
[2] N. Abelé *et al.*, *Electronics Letters*, Vol. 41, No 5, pp.242-244, 2005
[3] N. Abelé *et al.*, *Proc of IEDM 2005*, 19.6.
[4] H. Kam *et al.*, *Proc of IEDM 2005*, 19.2.
[5] S. Mahapatra *et al.*, *IEEE trans. on electron devices*, Vol. 51, No 11, pp.1772-1782, 2002.
[6] M. Kirihara *et al.*, *Jpn. J. Appl. Phys.*, Vol. 38, pp.2028-2032, 1999.
[7] COMSOL, User's guide; see also www.comsol.com.
[8] SmartSpice, User's guide; see also www.silvaco.com.

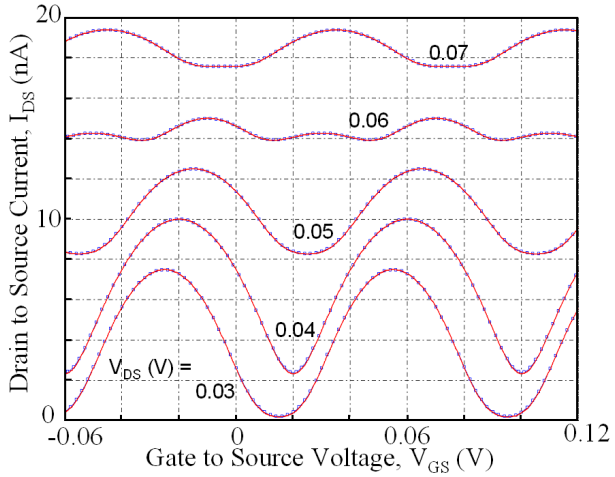

Fig. 1 I_{DS}-V_{GS} characteristics of our model (solid line) compared with EPFL's MIB model [2] (dotted line) for symmetric device with C_G=2aF, C_D=C_S=1aF and R_D=R_S=1MΩ, at T=15K.

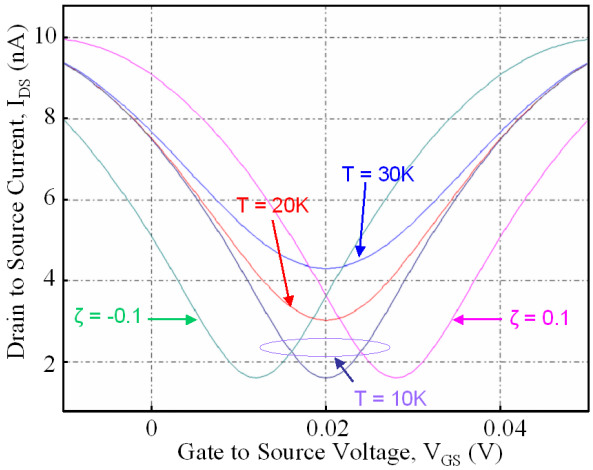

Fig. 2 I_{DS}-V_{GS} characteristics of our model at different temperature levels and for different background charge values for symmetric device with C_G=2aF, C_D=C_S=1aF and R_D=R_S=1MΩ, at T=15K.

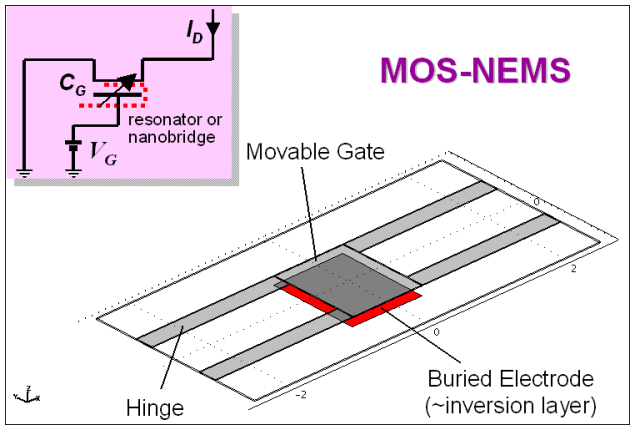

Fig.3 3-D simulation of a SG-MOSFET membrane with COMSOL [3].

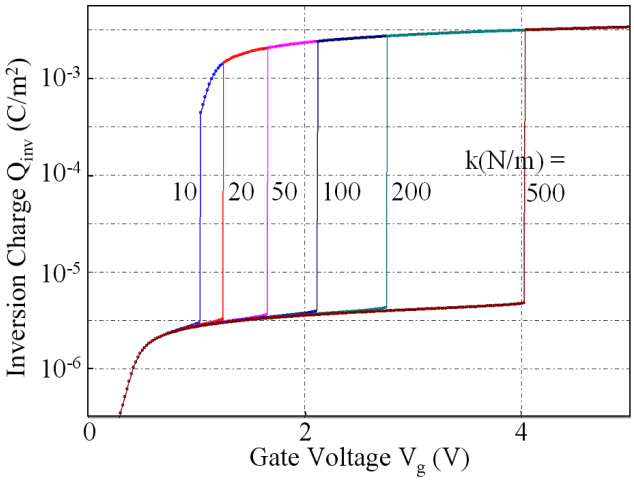

Fig. 4 SG-MOSFET inversion charge Q_{inv}, vs. gate voltage V_g, with spring constant, k, as a parameter.

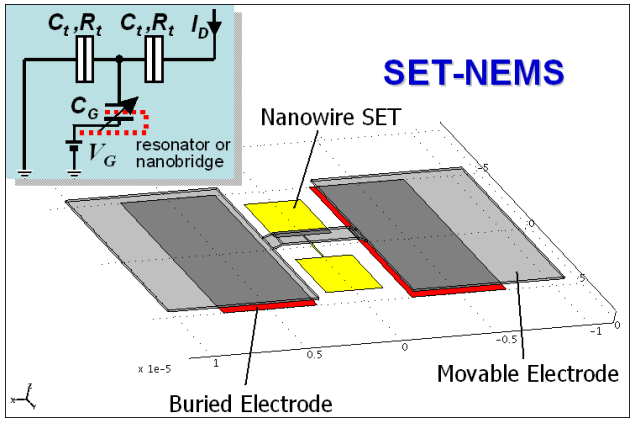

Fig. 5 3-D simulation of a SET-NEMS movable gate with COMSOL [3].

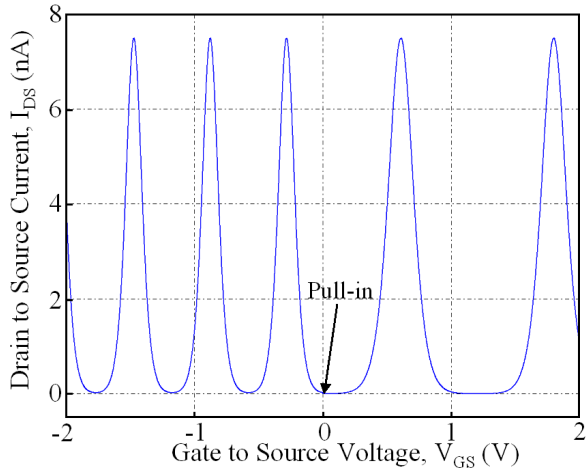

Fig. 6 SET-NEMS drain to source voltage I_{DS}, vs. gate to source voltage V_{GS}, with pull-in effect occurring at V_{GS}=0V.