Fabrication and evaluation of Si nanobridge transistor

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1 introduction

The ITRS2005 predicts that the CMOS miniaturization trend will be pursued further, and the physical gate length will reach under 10 nm long in the next decade. Along with the CMOS trend, various nanoelectromechanical systems (NEMS) have recently been developed by making the characteristic length (such as the resonator length) shorter in an attempt to increase their operation frequency. For example, the oscillation frequency of over 1 GHz has been for the 1.1-μm-long SiC based beam [1]. By downscaling the structures towards the 100-nm regime, we may explore new properties of Si NEMS structures. For example, we expect phonons and electron-phonon interaction in a nanoscale bridge structure, which is acoustically isolated from the Si substrate, to show different properties from those in bulk Si. In addition, by combining the nanobridge (1D) structures with nc-Si dot (0D) structures, new electromechanical phenomena may emerge. This may include ones such as a phononic bandgap & phonon confinement [2] a reduction of electron-phonon interaction [3][4], the phonon blockade [5], metal-insulator transition, quantization of nanomechanical motion [6], and a strong coupling of nanomechanical and electron motions [7]. These may lead to novel functional Si nano information devices [8] which are not achieved by using the conventional bulk Si CMOS technologies.

2 Si nanowire and nanobridge transistors

Figure 1 shows schematic device structure of our Si nanobridge (SiNB) transistor. We first patterned a Si nanowire (SiNW) channel and double side gates on either a heavily-doped thin SOI or nanocrystalline Si film.

The SiO_2 layer under the channel was then etched out, and a suspended nanobridge channel was formed, which is free from the substrate. It is well known that heavily-doped Si nanowires exhibit single-electron charging effects because of the electron islands and tunnel junctions naturally formed in the SiNW due to random-dopant-induced potential fluctuation [9]. In the SiNW formed on the nc-Si film, the nanocrystalline Si grains and grain boundaries act as a charging island and tunneling barrier, respectively [11]. The electrostatic potential of the charging islands in the SiNWs is modulated by applying the gate bias to the double side gates. For the SiNB channels with a certain air gap from the substrate, we expect that the stray capacitance between the charging island and the substrate becomes negligibly small, and therefore the Coulomb blockade phenomenon can be observed at higher temperatures compared with the SiNW channel SETs. We also expect for the SiNB that the tunneling current may be modulated based on the mechanical deformation of the SiNB if the dimensions of the SiNB are small enough and the electrostatic force caused by the side gate bias is large enough.

3 Fabrication of Si nanobridge transistors

We fabricated SiNB transistors with various channel length, width and thickness on thin SOI layers with phosphorous doping of about 10^{20}cm^{-3}. We first pattern the SiNW channel and double side gate by EB-lithography and anisotropic ECR-RIE dry etching. After that, the buried oxide layer under the SiNW was etched out by using HF wet etching.

Figure 2 shows the SEM image of the fabricated SiNB transistor with the channel length of 1μm, width of 400nm and thickness of 100nm. It turns out that both the SiNB channel and double side gates are bent downwards and the tip of the gate fins almost touches the Si substrate. This is presumably caused by surface tension of water during the drying process after the wet etching. We would need to use the super critical drying technique to solve this problem. However, we found that such cumbersome problems disappear by optimizing the device layout and making the whole structures smaller. Figure 3 shows the SiNB transistor with the length of 400nm, width of 50nm, and thickness of 50nm. We adopted a wider side gate pattern which controls the overall SiNB channel potential. The SiNB did not show any downward bending despite the NB thickness of only 50 nm. Compared with the SiNB shown in Fig.2, all the NB dimensions are scaled down about a half, but the surface tension is expected to be much smaller as the surface area of the NB decreases.

4 SiNW and SiNB SET characteristics

We first characterized the fabricated SiNW transistors formed on a 50-nm-thick SOI substrate. Figure 4 shows the I_{ds}-V_{gs} characteristics measured at temperature of 20K when the common gate bias was applied to the double side gate. We observed Coulomb oscillation of the current with a large oscillation period of about 6 V, which indicates a single charging island formed in the SiNB dominates the oscillation. The Coulomb oscillation persisted up to about 40K and washed out above that.

We then characterized the SiNB transistors by underetching the SiO_2 layer of the SiNW transistors measured above. Figure5 shows the I_{ds}-V_{ds} characteristic of the SiNB transistor at 150K. The inset shows the I_{ds}-V_{ds} characteristics for the SiNW transistor measured at 150K before underetching. By comparing these characteristics, the SiNB exhibits large nonlinearity while the SiNW transistor shows very linear characteristics. We suppose that this is because the stray capacitance between the charging island and substrate is virtually zero as mentioned above and also because the dimensions of the charging island get smaller as a result of natural oxidation from surrounding surface of the SiNB.

Figure 6 shows I_{ds}-V_{ds} characteristics of SiNB transistor measured at higher temperatures from 150K to 300K. The SiNB transistors showed very large temperature dependence of the current compared with that for the SiNW transistors (the inset to Fig.6). Figure 7 shows the Arrenhius plot, $\ln(\sigma)$ v.s. $1/T$. We estimated the effective barrier height of the tunnel barriers E_B by using the almost linear regions at high temperatures and obtained E_B of 217 meV. This value of the barrier height seems to be large enough to observe the single-electron charging effects at high temperatures [11]. In contrast the E_B evaluated for the SiNW transistors was 19.6 meV, which is consistent with much lower operating temperatures of SiNW SETs shown above. This indicates that natural surface oxidation of the NB works not only for making the charging island smaller but also electron confinement stronger in the SiNB channels.

Refarences

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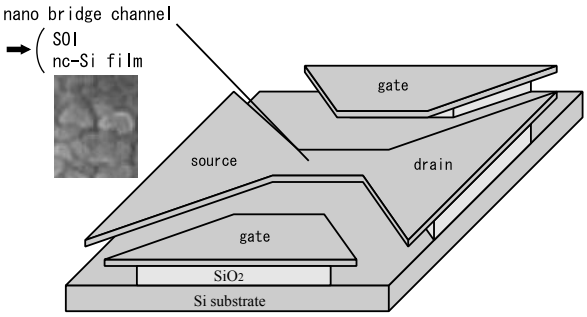

Fig.1 Device structure

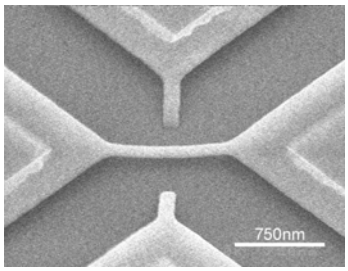

Fig.2 SEM image of SiNB. Length is 1μm, width is 400nm and thickness is 100nm.

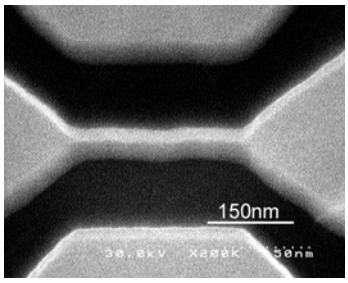

Fig.3 SEM image of SiNB. Length is 400nm, width is 50nm and thickness is 50nm.

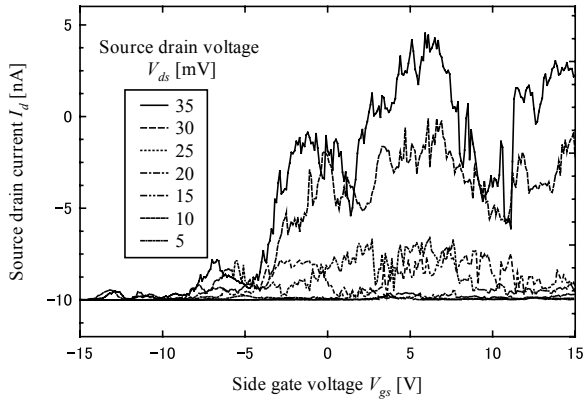

Fig.4 I_{ds}-V_{gs} charcteristics of the SiNW transistor measured at tempreture of 20K

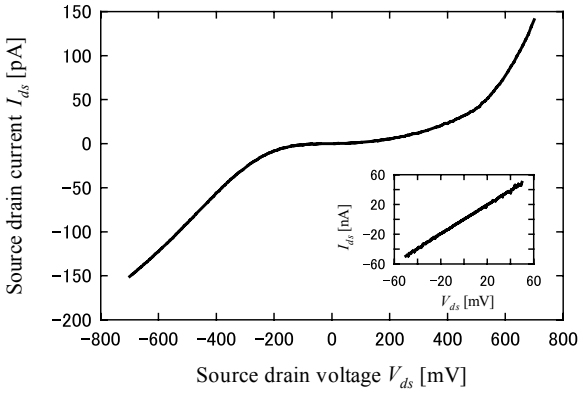

Fig.5 I_{ds}-V_{ds} characteristics of the SiNB transistor measured at 150K The inset shows I_{ds}-V_{ds} characteristics for the SiNW transistor measured at the same tempreture.

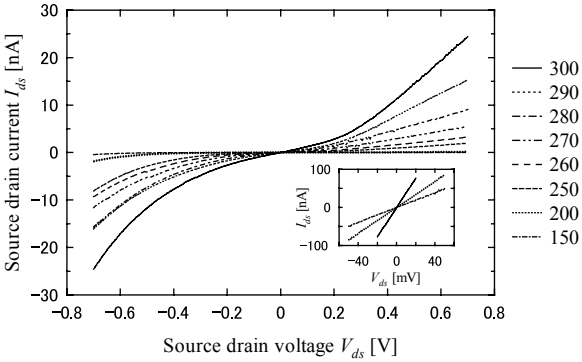

Fig.6 I_{ds}-V_{ds} characteristics of SiNB transistor measured at higher tempreture from 150K to 300K. The inset shows I_{ds}-V_{ds} characteristics of SiNW measured at the same tempreture.

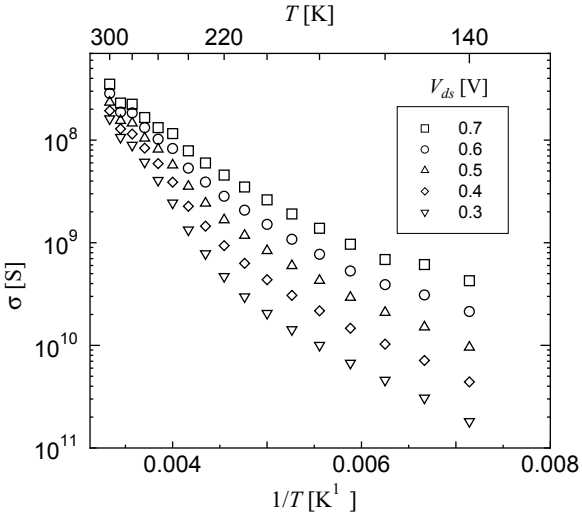

Fig.7 Dependence of the log of the nano bridge conductivity σ on the inverse tempreture $1/T$.