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Charge storage in silicon nanocrystals and device application

S. Oda, S-Y. Huang, M. A. Salem, and H. Mizuta

Tokyo Institute of Technology, Tokyo 152-8552, Japan
E-mail: soda@pe.titech.ac.jp

Single-electron tunneling and charge storage in silicon nanocrystals are discussed with reference to non-volatile memory device application. Silicon nanocrystals are prepared by very-high-frequency plasma decomposition of silane. Coulomb blockade and oscillation is observed in both planar and vertical structure transistors. Discrete charge storage is observed in silicon nanocrystals floating gate memory devices. Macroscopic charging properties in floating gates are characterized by capacitance and conductance measurements. Microscopic charging properties are investigated by Kelvin probe force microscopy. Quantized electron charging is observed. Memory retention characteristics are improved by dual memory nodes using surface nitrided silicon nanocrystals.

1. Introduction

Three-dimensionally confined silicon nanocrystals (Si-NC) have been investigated extensively over the past decade for their promising applications in novel nanoelectronic devices. New functions in electron transport, photon emission and electron emission are feasible due to quantum confinement of electrons and charges in nanostructures and large interactions between nanocrystals even at room temperature [1]. In our previous works, Coulomb blockade and oscillation were observed in both planar and vertical structure transistors using Si-NCs as Coulomb islands [2,3]. Discrete charge storage was observed in Si-NCs floating gate memory devices even at room temperature [4,5]. Flash-type memory devices, with a continuous layer of nitride as a floating gate, are widely used as non-volatile memory application. Si-NC based memory features in electrically isolated charge-storage nodes in an oxide film as a floating gate, where charge leakage through localized oxide defects could be greatly reduced. Consequently, performance reliabilities as well as the memory retention characteristics should be improved. This implies that much thinner tunneling oxide layer can be employed resulting in lower operating voltage and faster switching time compared to conventional flash-type devices. If we can control a single or a few electrons in a memory node based on the Coulomb blockade effect, novel functions such as multi-value memory or a very low-power consumption devices become possible

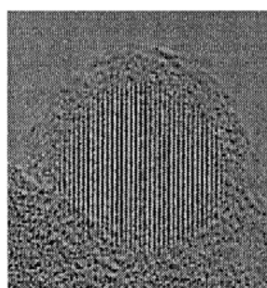
Charge injection and storage in dense arrays of Si-NCs in SiO_2 is a critical aspect of the Si-NC memory performance. Any incremental change in the very small number of total electrons in a collection of Si-NCs leads to a significant shift of the Si-NC energy levels relative to the band edges of the nearby semiconductor channel. For such nanometer-scale semiconductor nanocrystals, the electron wavelength may approach the dimension of the nanocrystals, under which condition the quantum confinement energy may become comparable to both the electron charging energy and the thermal energy at room temperature. Therefore, comprehensive understandings of electron storage correlated with

Coulomb charging and quantum confinement effects in such few-electron systems may enable to benefit forthcoming device applications.

In this article, we discuss electron charging, storage and discharging in Si-NCs through a combination of charge measurement experiments. Capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) characteristics were measured for MOS diodes with arrays of Si-NCs as a floating gate. Atomic force microscopy (AFM) and Kelvin probe force microscopy (KFM) methods were applied to individual dots to obtain a microscopic picture of charge storage in Si-NC.

2. Experimental

Si-NCs investigated in this work are prepared by a unique method to obtain uniform size by separating and manipulating the nucleation and crystal growth processes in very high frequency plasma decomposition of silane (SiH_4) and coalescence of radicals [6]. Thus prepared Si-NCs can be a mono-layer with diameter of 8 nm as well as narrow size distribution of ±1 nm. Fig. 1 shows a high-resolution transmission electron microscope (HRTEM) image of the Si-NC surrounded by natural oxide. A spherical particle is clearly observed. The lattice image clarifies that the ultra-fine particle is a single-domain crystal. A thin layer of surface oxide serves as an ideal potential barrier, which confines electrons effectively, as well as a tunnel barrier and terminators of interface dangling bonds. Silicon nitride can be an alternative tunnel barrier. Direct nitridation method using plasma driven atomic nitrogen provides a thin layer of high-quality nitride which covers Si-NCs.



10nm

Figure 1: HRTEM image of silicon nanocrystal

A memory device using a SiO_2/Si-NCs/SiO_2/Si-substrate structure has been demonstrated to be a simple and efficient model for investigation of electron charge/storage/discharge mechanisms in Si-NCs identified through *C-V* and *G-V* spectrum [7]. Average effects from a large number of Si-NCs under an electrode with diameter of 100 μm can be explored. Trapping/detrapping processes in Si-NCs, oxide defects and interfacial defects were identified through *C-V* and *G-V* spectrum with varying temperature or frequency during voltage-dependent measurements. The electronic properties of Si-NCs, including Coulomb charging and quantum confinement effects were extracted from combination of *C-V* and *G-V* measurements [8].

On the other hand, in order to examine the charge storage in nano-scale area, an AFM based KFM method was employed. Topographic and potential images of Si-NCs were measured simultaneously by using a rhodium coated silicon cantilever. The transient contact potential difference (CPD) for Si-NCs obtained by such a method can be used to investigate the diameter dependent charging energies with a single and few electrons storage. We are able to estimate the amount of charge quanta stored in each individual nanocrystal directly.

Recently we succeeded in estimating the number of electrons stored in the individual nanocrystals by analyzing the measured CPDs [9].

3. Charge Storage Characteristics

A major essential issue for Si-NC memory devices in nonvolatile memory applications is the data retention characteristics over extended period of time. In this work, we studied two kinds of Si-NC: without surface nitridation (sample A) and surface nitrided (sample B). A floating-gate of memory devices with a SiO_2 (41 nm)/{Si-NC or nitrided Si-NC}/SiO_2 (1 nm) dielectric-layer on a <100> oriented p-type silicon substrate (8 ~ 10 Ω·cm) has been chosen for these studies. The Si-NC density is about 1.1×10^{11} cm^{-2}. Fig. 2 shows the schematics of the sample B comprising Si-NCs surrounded with thin silicon nitride films of 1 nm in thickness. The detailed fabrication processes were described elsewhere [10].

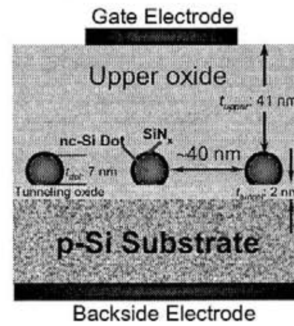


Figure 2: Structure of surface nitrided silicon nanocrystal floating gate

As shown in Fig. 3, a clear hysteresis in *C-V* curves is found at the flat-band voltage shift (ΔV_{FB}) of 0.196 V in sample *A*, when we swept the voltage between inversion and accumulation regions at room temperature. It is interesting to point out that the significant increase of the memory window of *C-V* characteristics of ΔV_{FB} = 0.372 V can be found in sample *B*. It is worthwhile to point out that the observed hysteresis in *C-V* curves can solely attributed to charge stored in Si-NCs since no hysteresis can be observed in control samples without dot deposition. The enlarged memory window implies that traps in surrounding silicon nitride films can offer extra carrier trap sites and thus enlarge the flat- band voltage shift in the memory operations. In other ward, in nitrided Si-NCs, charges could be stored in not only Si-NCs but also in trap-states of silicon-nitride films.

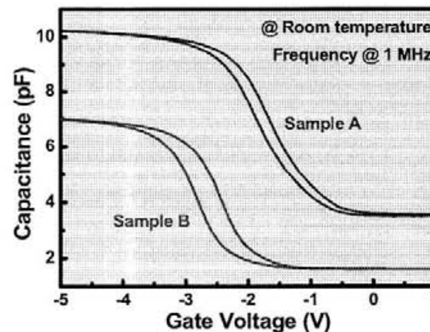


Figure 3: C-V Characteristics of Si-NC (A) and nitrided Si-NC (B) based memory devices

After some electrons are trapped, at a chosen reading voltage (e.g. flat-band voltage), the stored electrons have a finite probability to tunnel back to the substrate, which could cause a gradual shift of the structure capacitance. These gradual shifts directly reflect

barrier heights/widths, internal electric fields, defect or interfacial states, and so on. Therefore, investigations of time dependences of memory windows as well as charging/discharging behaviors of Si-NCs correlated with Coulomb blockade and quantum confinement effects offer better understanding of retention characteristics of Si-NC memory devices. In this work, after the memory nodes were filled with electrons at a write-voltage of +3 V, the capacitance was measured at the initial flat-band voltage of –1.6 V and –2.4 V for samples *A* and *B*, respectively. The measured capacitance is converted to be a ratio of the stored charge to the initial stored-charge, as shown in Fig. 4. Three orders of the magnitudes increase in the retention time were observed in sample *B* compared to those using Si-NCs only. Apparently, a remarkable long-term retention time is achieved using dual memory nodes: Si-NCs and traps of silicon nitrides.

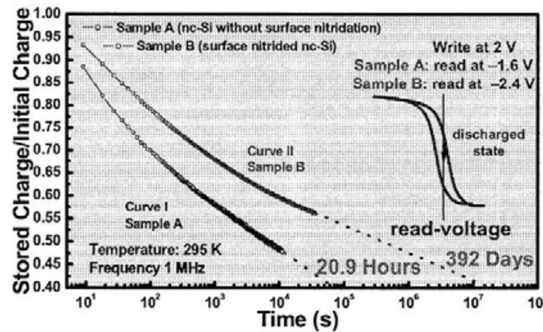


Figure 4: Memory retention characteristics for Si-NC with and without nitridation.

It is notable that curve *II* can be fitted into two straight lines, the charge-loss rate of the first part is larger than that of the second part, which implies that the discharging mechanisms are different for each of the linear parts. As is discussed above, the remaining and localized charges may be attributed to some of the charges falling into the traps of silicon nitrides and failing to tunnel back directly to the channel because of the higher thermionic barrier. The difference of the charge-loss rate between samples *A* and *B* could be due to the difference of charge storage-sites: Si-NCs for the former and Si-NCs/traps for the latter. We suggest that the first discharge part of sample *B* may result from the electrons stored and delocalized entirely over the Si-NCs, where the shorter distance apart from the channel and delocalized states may lead to a higher charge-loss rate, as what occurred in sample *A*. The discrepancy that the charge-loss rate of sample *A* is slightly greater than that of the first part of sample *B* may result from much larger number of electrons stored in the Si-NCs in sample *A*, while some of the stored electrons falling into nitride traps in sample *B*, thus reducing the number of delocalized electrons. Moreover, the second discharge part may result from the localized charges in the nitride traps on top of the Si-NCs, where the longer distance apart from the channel and localized states (thermionic barrier) lead to a smaller charge-loss rate. Apparently, the technique of nitrided Si-NCs manifests themselves a prospective candidate for memory floating-gates toward nonvolatile memory device applications with maintaining fast operations.

On the other hand, in order to examine the charge storage in nano-scale area, an AFM conducting-tip with a radius of several tens of nanometer was employed to inject localized charge and map topographic as well as potential images, performed by an AFM based KFM mode. The investigated sample is sparsely distributed Si-NCs on a thin SiO_2 film, grown over a p-type (111) silicon substrate. Diameters of Si-NCs range from 2 to 8 nm.

Charge injection into the Si-NCs was carried out using the biased tip in the contact mode. After positioning the conducting tip to the targeted point, the tip was biased at -5 V

and was then edged nearer to the surface and kept in contact for 30 seconds. Then fifteen successive non-contact mode KFM scans (five minutes spent by per scan) were performed in order not only to observe the immediate effect just after charging, but also to observe the time-dependent change in the charged states of the Si-NCs. The additional charged electrons will give rise to increase the overall Si-NC potential. The change in the measured CPD of the Si-NCs shows the charging energy of the individual nanocrystals. Fig. 5 shows the simultaneously scanned topography and potential images (a) before and (b) after charging.

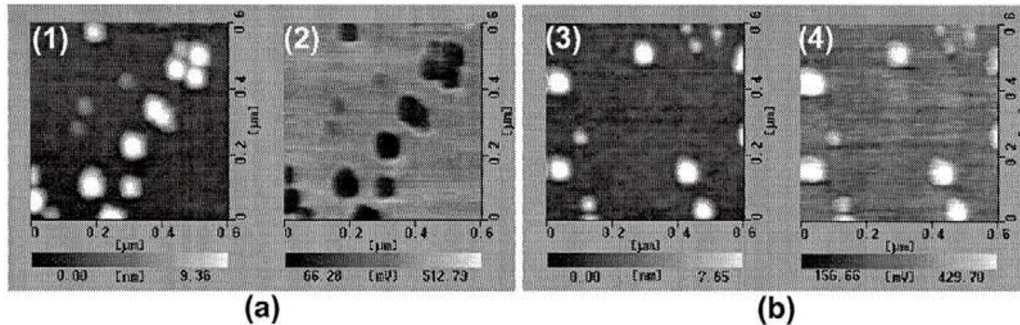


Figure 5: AFM and KFM measurements (a) before and (b) after charging. (1) and (3) are topography; (2) and (4) are potential images.

Note that the lateral nanocrystal dimensions are overestimated as the AFM image is given as convolution of the sample and tip shapes. However, we may obtain the diameter of the individual nanocrystals precisely from the vertical topography data since nanocrystals are spherical. The change in the nanocrystal spatial distribution after the charging may be attributable to the repulsive forces between the charged nanocrystals. In the potential image (Fig. 5(2)), the clear distinction between the Si-NCs and the substrate is observed. In addition, we see that the larger Si-NCs tend to show the lower potential. As expected, in Fig. 5(3), the topographic height did not show any significant change after the charging since the KFM measurement system cancels the electrostatic forces between the tip and the sample. In Fig. 5(4), it is interesting to note that larger Si-NCs show higher potential than that for smaller Si-NCs. This gives an indication that the larger Si-NCs have been highly affected by the charging process comparing with the smaller Si-NCs, while the substrate remains at almost the same potential of about 300 mV. This manifests that only the Si-NCs were charged and that the KFM facilitates to detect the charge confined dependence of the size in the nanostructures experimentally.

The number of electrons injected into each nanocrystal can be estimated by comparing the measured CPD change with the charging energy, $E_c = (ne)^2/C_{dot}$, where C_{dot} is Si-NC capacitance and n is the number of injected electrons. Fig. 6 plots the Si-NC CPD change as a function of its diameter, along with the charging energy calculated with one, two and three extra electrons per nanocrystal for (a) the first potential scan after the charging and for (b) the fifteenth scan after charging (after 75 min.). Fig. 6(a) shows that only one electron is stored in the Si-NC with diameter up to 2.8 nm, and three electrons are stored in the Si-NCs with diameter in the range from 4.7 nm to 7.4 nm. The Si-NC with a diameter of 4.6 nm likely stores two electrons. Fig. 6(b) shows that there is one electron loss occurred after 75 minutes to all the larger Si-NCs (with diameter range from about 4.8 to 7.4 nm): the charge quanta decreased from three to two. On the other hand, the smaller Si-NCs did not show such loss of electrons, which means that they are able to preserve the stored charge at

least for the present measurement period. As our best knowledge, present results are the first direct measurement of the size-dependent potential of the individual Si-NCs. The method is useful to understand the mechanism of the leakage current in the Si-NC flash memory.

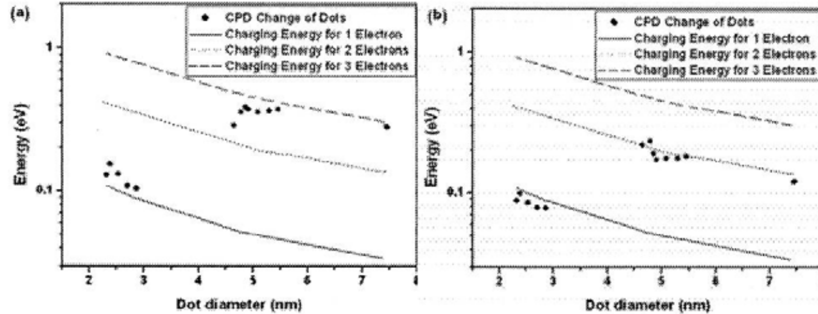


Figure 6: Charging induced change of differential surface potential in Si-NC with various sizes for (a) 5 min and (b) 75 min after charging.

4. Summary

We studied charge storage in Si-NCs in terms of non-volatile memory device applications. Macroscopic charging properties in floating gates involved millions of Si-NCs are characterized by *C-V* measurements. Charge storage is identified by means of *C-V* hysteresis and remarkable improvement in memory retention characteristics is experimentally demonstrated approachable by dual memory nodes using surface nitrided silicon nanocrystals. Microscopic charging properties involved individual Si-NCs are investigated by KFM. The number of injected electrons has been identified by comparing the measured CPD changes as a function of the Si-NC diameter. Quantized electron charging is observed. Both of these methods may provide a powerful tool for investigation on local electronic states and transport properties in the modern nanoelectronic devices.

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