

Energy-Balance Modeling of Short Channel Single-GB Thin Film Transistors

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INTRODUCTION

Polysilicon has been proposed as a possible candidate for a device material for thin film transistors for use in 3D VLSI circuit designs [1]. It is simple to use solid phase crystallization of deposited amorphous silicon to fabricate poly-Si films. This technique results in grain sizes of the order of hundreds of nanometers or less, which is comparable to the channel length and therefore only a single GB may be present in the channel. Although the GB is detrimental to the mobility of the TFT, in [2] we showed that the potential barrier formed at the GB can assist in lowering the device off-current. Previously our simulation method used a simple drift-diffusion based transport model. We aim in this study to validate the results in [2] by using a more realistic model. Therefore we use a calibrated energy transport model and a continuous trap state distribution at the GB.

SIMULATION METHOD

The device structure used in the simulations is shown in Fig 1, where the shading denotes the doping concentration. Shockley-Read-Hall statistics are used to model the trapping mechanisms at the GB and the trap distribution is continuous with a peak close to midgap.

For accurate simulation of devices in the deep submicron regime, an extended drift-diffusion model derived from the higher order moments of the Boltzmann equation is used. This energy balance model, incorporates carrier temperature/energy, as a further transport parameter, and consists of a set of six coupled partial differential equations. These are for energy balance, current density and energy flux for both holes and electrons respectively.

The energy relaxation time for electrons and holes is a critical parameter in the energy balance equations. It is a measure of the amount of time needed for the carrier energy to reach equilibrium with the electric field. The larger the relaxation time then the greater the magnitude of any non-stationary effects.

The value of the relaxation time is controversial, as it is not directly measurable, and incorrect values can lead to non-physical behaviour in the simulations. Furthermore, the relaxation time is not constant but

simulations to evaluate the ensemble average value. The extracted relaxation time for electrons against carrier energy is plotted in Fig. 2, along with a curve fitted using an arbitrary function.

SIMULATION RESULTS

Both a single-GB TFT and an SOI equivalent were simulated under the bias conditions of $V_d=0.01V$ and $1.2V$. A comparison of the I_d - V_g characteristics when using the DD model and the calibrated energy balance (EB) model is shown in Figs 3 and 4. The drain currents calculated using the EB model are higher than those when using the DD model. This can be explained by considering the velocity overshoot effect. As previously discussed velocity overshoot is the consequence of the finite time needed for the energy of the carriers to return to their equilibrium values. If we compare the electron velocity at 1nm from the semiconductor/oxide interface (Fig. 5), we see that the carrier velocity is much higher, when using the EB model.

To investigate if lower off-state current in the single-GB TFT is still found when using the EB model, devices were simulated with channel lengths of 100nm, 75nm, 65nm and 53nm. The I_d - V_g characteristics are shown in Figs 7 and 8, for $V_d=0.01V$ and $1.2V$ respectively. In both instances the single-GB TFT shows better immunity to short channel effects than the SOI equivalent. To summarise this behaviour we plot threshold voltage, V_T , as a function of channel length, L (Fig. 6). The threshold voltage roll off is clearly larger for the SOI equivalent device.

CONCLUSIONS

We therefore can conclude that the results reported in [2] regarding improved off-state current are valid even when non-equilibrium transport is considered in the simulation model.

- [1] K. Banerjee, *et al.*, Proceedings of the IEEE 89(5), pp 602, 2001
- [2] P. Walker, *et al.*, IEEE Trans. Electron Devices, 51(2), pp 212, 2004

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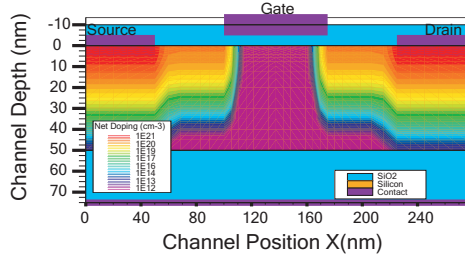


Figure 1: The device structure used in the energy balance simulations. The contour shading denotes the net doping and shows the lightly doped drain (LDD) structure utilised in the device.

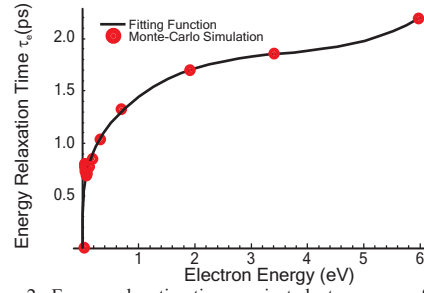


Figure 2: Energy relaxation time against electron energy for intrinsic silicon. An arbitrary function was fitted to the data points supplied by a Monte Carlo simulation to model the temperature dependence of the relaxation times.

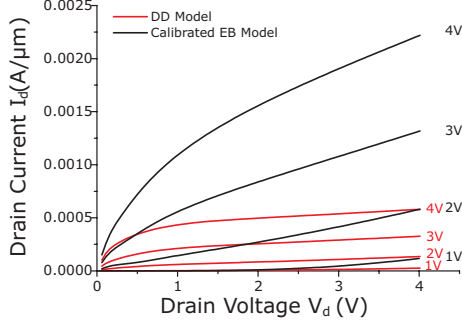


Figure 3: An overlay of the I_d - V_d characteristics at $V_g = 1V, 2V, 3V, 4V$ for a 100nm single-GB TFT. Comparison between the results from the drift-diffusion (DD) model and the calibrated energy balance (EB) model show that larger drain currents result when the EB model is used.

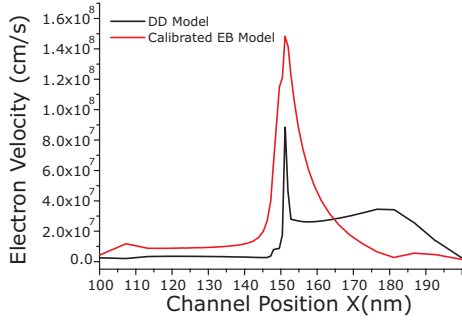


Figure 5: A comparison of the electron velocity in the channel ($V_d = 1.2V$, $V_g = 3V$ and $L = 100nm$) when using the drift-diffusion (DD) or calibrated energy balance (EB) model. The max electron velocity is higher when using the EB model due to the velocity overshoot effect.

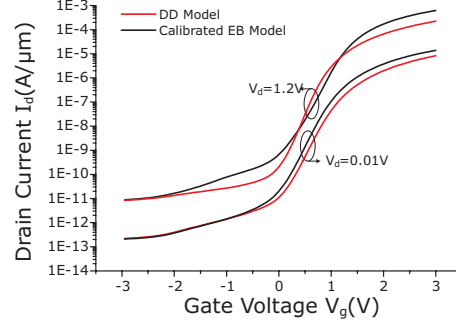


Figure 4: An overlay of the I_d - V_g characteristics at $V_d = 0.01V$ and $1.2V$ for a 100nm single-GB TFT. A comparison is made between the results from the drift-diffusion (DD) model and the calibrated energy balance (EB) model.

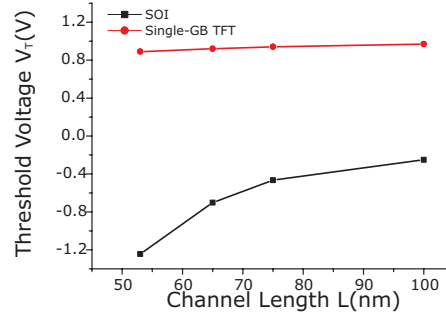


Figure 6: Threshold voltage as a function of channel length for a 100nm single-GB TFT and SOI equivalent when $V_d = 0.01V$.

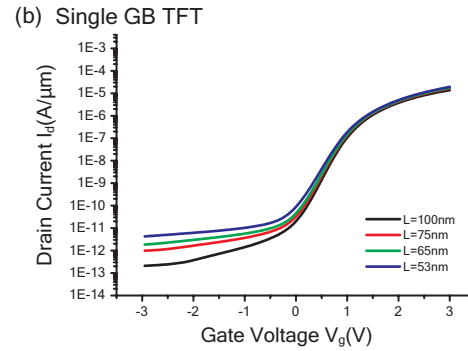
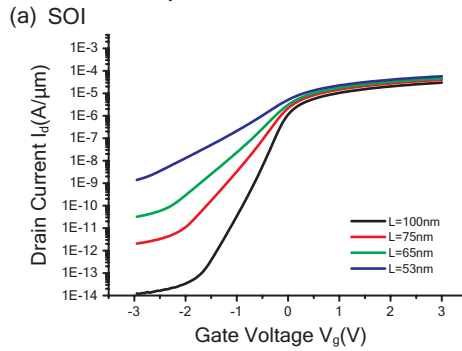


Figure 7: I_d - V_g characteristics at $V_d = 0.01V$ for (a) SOI (b) single-GB TFT using the calibrated energy balance model. The GB suppresses the off-state current and hence the single-GB TFT has better subthreshold behaviour.

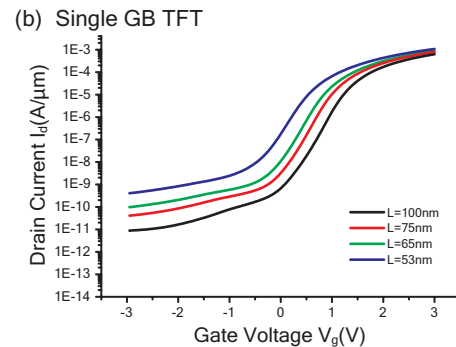
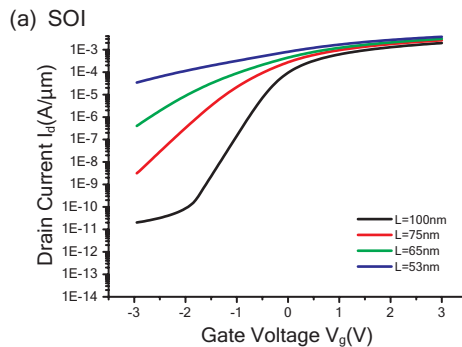


Figure 8: I_d - V_g characteristics at $V_d = 1.2V$ for (a) SOI (b) single-GB TFT using the calibrated energy balance model. The subthreshold degradation in the SOI device becomes severe at the increased drain bias whereas the single-GB TFT shows good DIBL immunity.