

Electronic states and quantum transport in Si nanorod transistors

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Introduction

The ITRS foresees the gate length of MOSFETs will be reduced towards 10 nm in the next decade. Along with such an aggressive downscaling, the bottom-up approach is also getting more interest to fabricate Si nanodevices, which adopts Si nanorods (SiNRs) with diameter of a few nanometer as a building block [1,2]. A thin film transistor has been fabricated with assembled SiNRs as a channel, and the carrier mobility as high as those for the conventional MOSFETs has been demonstrated [3]. Since assembly of the SiNRs can be performed on non-Si substrates such as glass and plastic, the Si-based bottom-up approach may lead to high-performance and large-area electronics.

As the diameter of the SiNRs is reduced, the effects of Si surface atoms on the entire properties will be more important, and the quantum size effects are expected to be remarkable. Atomistic simulation is indispensable to clarify the electronic and transport properties of the SiNRs. In this work we adopt SIESTA[4,5], which is a DFT based *ab initio* simulation for calculating the electronic states of the SiNRs. We also introduce TransSIESTA [6], which solves the DFT and the nonequilibrium Green's function theory in a self-consistent manner for calculating transport properties for the SiNRs with nanoscale electrodes.

Quantum size effects in SiNRs

Figure 1 shows the SiNR structure used in the present analysis. All the dangling bonds on the rod surface are terminated by hydrogen atoms. We calculated Total Density of States (TDOS) and evaluated the band gap E_g from the HOMO-LUMO separation for the SiNRs with the diameter d less than 2 nm and with the length l of 2nm and 3 nm. The resulting E_g shows a dramatic increase with decreasing d due to the quantum size effects (Fig. 2), which is a similar trend to the recent experimental results reported for the SiNW [2]. An underestimate seen for the calculated E_g is attributable to the use of LDA (local density approximation) in the DFT and is more or less in common for such *ab initio* calculations.

Transport properties of a SiNR transistor

Figure 3 shows a SiNR channel sandwiched between Au(111) nanoelectrodes: l is varied from 4 to 12 nm. Figure 4 shows the l -dependence of transmission spectrum. For the 4 nm-SiNR the continuous transmission spectrum is observed without any gap, which implies metallic behaviors. On the other hand, for 8 nm and 12 nm the transmission spectra show a finite gap, namely semiconductor natures. Such transition from semiconductor to metallic behaviors with a decrease in l is consistent with the previous report on the Si atomic wires by Landman *et al.*[7]. The spatial electron distribution is visualized in Fig. 5 for the 8 nm SiNR at four characteristic energies. It shows clearly that the electronic states in the band gap exhibit a hybrid nature of the Si and Au orbitals.

Current-voltage characteristics calculated by using the transmission spectra (Fig. 6(b)) under finite source-drain voltages are shown in Fig. 6(a). It should be noted that the I-V curve for the 8 nm SiNR is nonlinear while that for the 4 nm SiNR is virtually linear, which are consistent with the above discussion. We also calculated the gate bias dependence of the current for the 4 nm SiNR transistor under the source-drain voltage of 1 V (Fig. 7(a)). A shift in the transmission band caused by the gate bias is indicated in Fig. 7(b). The transistor exhibits a clear current modulation via gate bias although the current is not pinched-off completely due to its metallic nature. Details of the SiNR transistor characteristics will be discussed.

Acknowledgement

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References

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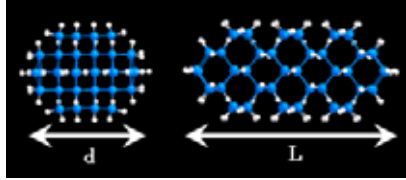


Fig.1: A SiNR structure used for the present analysis

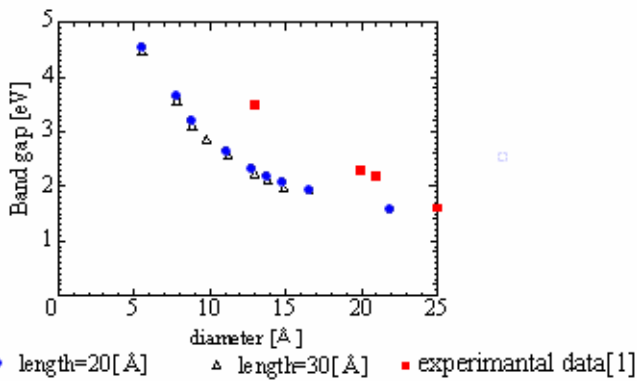


Fig.2: The band gap as a function of the SiNR diameter

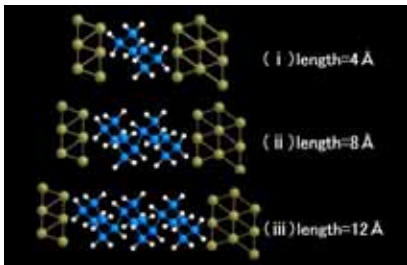


Fig.3: SiNRs with Au nanoelectrodes

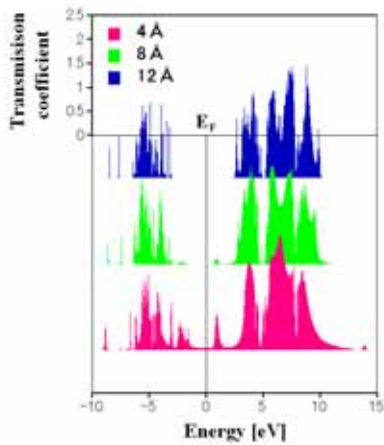


Fig.4: Transmission spectra for SiNRs with different length

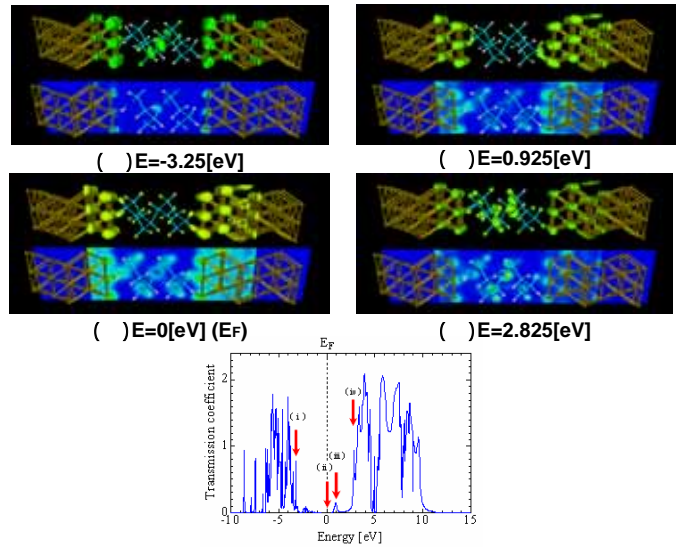


Fig.5: The DOS isosurfaces at four energies indicated by arrows

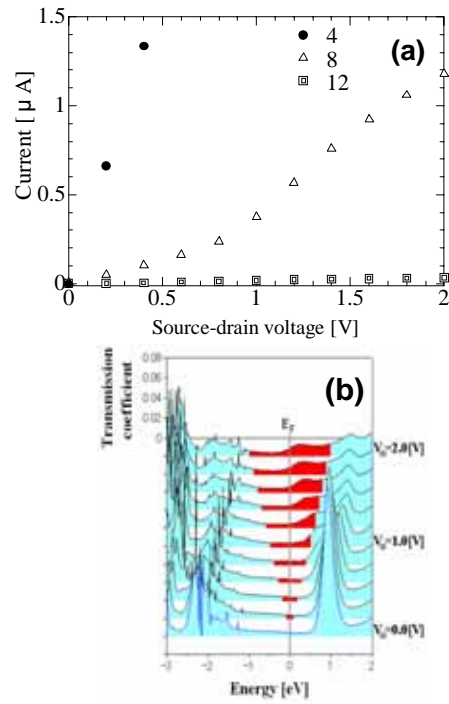


Fig.6: the calculated current of the Fig.3 model versus source-drain voltage

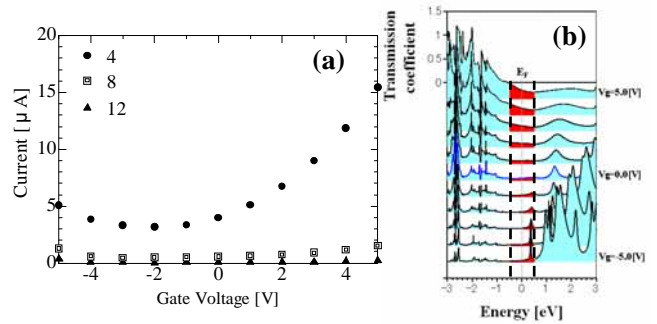


Fig.7: the calculated current of the Fig.3 model versus gate voltage