# Charging-Storing-Discharging Processes in Nitrided Nanocrystalline Silicon Dots

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## I. Introduction

Nanocrystalline silicon (nc-Si) memory devices have emerged as a descendant of flash memories beyond scaling barriers during the recent decade, where fast write/erase, long retention time and superior endurance with non-destructive read were demonstrated based on only a few or even single electron(s) [1]. However, since an ultrathin tunneling oxide film was involved for high-speed operations and charge storage in a floating gate essentially raises its potential, stored charge is easily released from memory nodes via direct tunneling. Therefore, nc-Si memory devices always encounter a dilemma between operation-speed and retention-time. In this work, we developed nitrided nc-Si dots as a candidate of memory nodes facilitating tradeoff for nonvolatile applications with fast operation speeds [2]. A long-term retention based on completely different storage- mechanisms is illustrated.

## II. Experimental

A capacitor memory device with a $SiO_2$ (41 nm)/silicon nitrides (1 nm)/nc-Si dots (7 nm)/$SiO_2$ (1 nm) sandwiched dielectric-layer on a <100> orientated p-type silicon substrate (8 ~ 10 Ω·cm) has been chosen to study electrical properties of nitrided nc-Si dots, as shown in Fig. 1. Three different samples were studied, denoted by *A* (nitrided nc-Si dots), *B* (as deposited nc-Si dot without nitridations), and *C* (no nc-Si dots but only nitridations on tunneling $SiO_2$), depending on the materials embedded among $SiO_2$ films.

Charge storage in the nitrided nc-Si dots as well as their charge-storage mechanisms were explored by means of displacement current-voltage (*I-V*) analyses. Since the displacement current, associating with time-varying voltage, is responsive to confined charges, it allows exploring charge or potential variations in embedded memory nodes [3].

## III. Results and Discussions

Figure 2 demonstrates that scan-speed dependences of the measured currents in sample *A* were consistent each other after normalizations. Therefore, the observed currents were the displacement current rather than the leakage current. The former is expressed as follows:

$$I_D = C_{MOS} \cdot \frac{dV_g}{dt} = C_{ox} \cdot \frac{dV_{ox}}{dt}, \qquad (1)$$

Here, $C_{MOS}$ is the total capacitance from dielectric layer and space-charge layer of channel, $V_g$ is the gate voltage, $V_{ox}$ is the potential dropped on sandwiched dielectric layers, and $t$ is the scan-time. The current peaks manifests the change of total MOS capacitance and of the potential change in the memory nodes.

In Fig. 3, *I-V* characteristics for Sample *A* were compared with those for Samples *B* and *C*. Neither direction-dependent current nor current peaks were observed in Sample *C*, as shown in Fig. 3(b). These indicate that (1) change of the total capacitance gives trivial contributions to the current, and (2) the nitrided $SiO_2$ films are unable to perform memory nodes. It is natural to attribute observed current peaks to the charge/discharge with memory nodes. In Fig. 3(a), a pair of charging and discharging current peaks with nc-Si dots was observed in Sample *B* with the same height and full width at the half maximum (FWHM). In Sample *A*, however, the height of the discharge peak is smaller than that of the charge peak. A smaller discharge current height implies that charge loss rate is smaller than charge injection rate in nitrided nc-Si dot operations, and the stored charge inside is not entirely released from the memory nodes at that certain voltage. Therefore, asymmetric pair current-peaks of Sample *A*, compared with symmetric ones of Sample *B*, are the direct evidence that stored charge in memory nodes were not only in nc-Si dots but also in silicon nitrides. Possible electron exchange between defect traps and nc-Si dots reduces charge loss rate and results in a decrease in current peak-height in the discharge processes.

Temperature dependences of *I-V* characteristics were measured at from 130 to 300 K, as shown in Fig. 4. Most notably, the height of charge current peak is remarkably raised and the discharge current evolves into two peaks located at –1.150 V (peak *I*) and –2.075 V (peak *II*) below 170 K, which responded to discharge from nc-Si dots and from silicon nitrides via nc-Si dots, respectively. The gate voltage spacing between these two neighboring peaks gives rise to a 117 meV potential-drop across a nitrided nc-Si dot. This energy could be understood as the energy difference between confined states of nc-Si dots and defect traps of silicon nitrides. The experimental estimation is consistent with a typical trap energy level in silicon nitrides [4], with considering band offset with respect to $Si/Si_3N_4$ system as well as quantum confinement effect in the nc-Si dots. The correlations between the nc-Si dots and defect traps of silicon nitride films are illustrated in Fig. 5. In the write process, electrons tunnele directly into nc-Si dots through ultrathin $SiO_2$ barrier and are confined in discrete bound energy levels of nc-Si dots. Evidently, fast operations could be obtained. For storage, besides some of charges in nc-Si dots, rest of stored charges drop into traps of silicon nitrides. In the erasure process, stored electrons in nc-Si dots first tunnele back to the substrate. Subsequently, stored electrons in silicon nitrides go back to nc-Si dots under a higher electric field, and then tunnele back to the substrate. Therefore, charging and discharging into/off nitrided nc-Si dots are dominated by nc-Si dots and silicon nitrides, respectively. These features enable the proposed memory nodes capable of nonvolatile memory applications with fast write processes. Erase-time could be improved using much thinner silicon nitride films in the tradeoff between storage and discharge processes.

## IV. Conclusions

The nitrided nc-Si dots offered dual memory nodes of nc-Si dots and silicon nitrides. Charge storage in such memory nodes was identified into two states, one was in delocalized state of entire nc-Si dots, and another was in localized state of defects in silicon nitride. The former provides fast write processes and the latter enables a long-term retention time. The nitrided nc-Si dots manifested themselves as a prospective candidate for the memory floating-gates toward nonvolatile memory devices applications to maintain fast operations.

## References

[1] S. Banerjee, S. Huang, T. Yamanaka and S. Oda, J. Vac. Sci. Tech. **B20**, 1135 (2002).
[2] S. Huang, K. Arai, K. Usami, and S. Oda, IEEE Trans. Nanotechnology **3**, 210 (2004).
[3] Y. Majima, Y. Oyama, and M. Iwamoto, Phys. Rev. B **62**, 1971 (2000).
[4] E. Lusky, Y. Shacham-Diamand, A. Shappir, I. Bloom, and B. Eitan, Appl. Phys. Lett. **85**, 669 (2004).

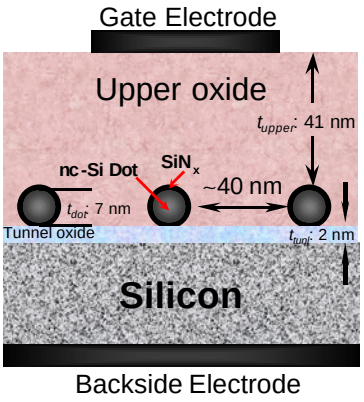



**Fig. 1** Si/SiO$_2$/nitrided nc-Si/SiO$_2$ capacitor memory devices. nc-Si dots were covered with silicon nitride films around 1 nm

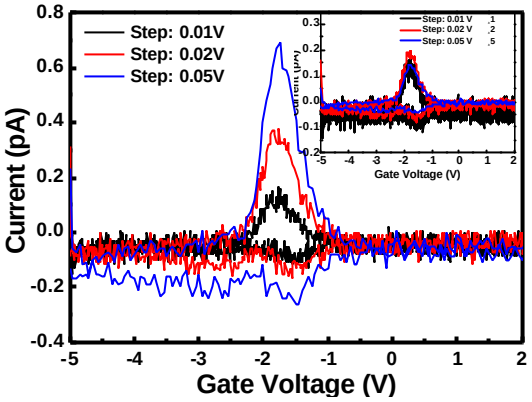
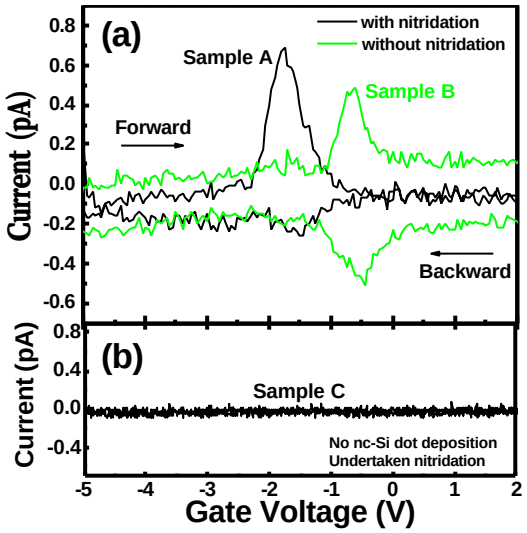



**Fig. 2** Gate-voltage scan-speed dependences of the measured displacement currents. Inset were normalizations upon scan speeds.



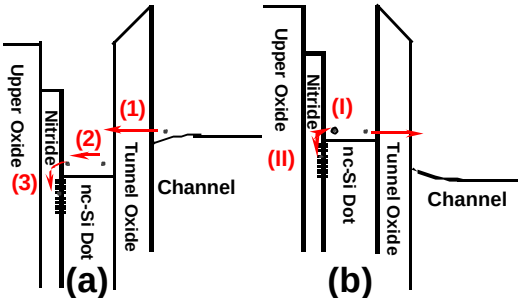




**Fig. 5** illustrations of (a) write and (b) erase processes in nitrided nc-Si dot based memory devices. (1) direct tunneling from channel to nc-Si dot; (2) polarization to the top of dot; (3) drop into defect traps of silicon nitrides; (I) delocalized states in nc-Si dots; (II) localized states in defect traps.

**Fig. 3** Displacement current characteristics of samples under identical gate-voltage scan-speed at room temperature. (a) Charge/discharge current peaks of samples *A* and *B*. (b) Nothing observed in Sample *C*.

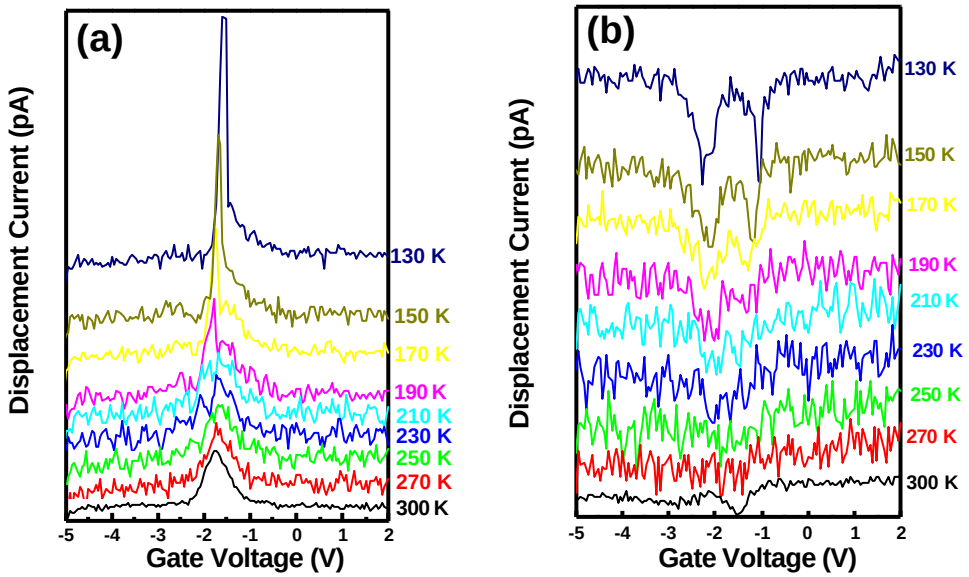



**Fig. 4** (a) charge and (b) discharge displacement current spectrum with temperatures.