Variation of Electrostatic Coupling and Investigation of Single Electron Percolation Paths in Nanocrystalline Silicon Cross Transistors

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Nanocrystalline silicon devices are promising candidates for the development of quantum-dot (QD) and single-electron transistors (SETs) compatible with large-scale integration processes [1]. These devices use nanocrystalline silicon materials where nanometre-scale crystalline silicon grains 'naturally' form large numbers of silicon QDs, isolated by tunnel barriers formed at thin amorphous silicon or silicon oxide grain boundaries. The small grain size leads to large electron-confinement and single-electron charging energies, raising the possibility of room-temperature operation of QDs and SETs [2]. The grain boundary tunnel barrier isolating the grains is also of great importance, as this determines the extent of the electrostatic and tunnel coupling between different grains. These effects can lead to the nanocrystalline silicon thin film behaving as a system of coupled quantum dots [3, 4].

A novel nanocrystalline silicon 'cross' transistor (Fig. 1) with four in-plane side gates, centre region (approximately 100 nm × 100 nm × 40 nm in size) and four leads (terminals) have been used to study the variation of electrostatic coupling between the grains (10 nm to 35 nm), and to estimate the locations of dominant charging grains along the various current percolation paths at a temperature of 4.2 K. This device allowed us to investigate the transition in the conductance through a few grains to conductance through a larger number of grains (Fig. 2). Under an extensive characterization of the currents through the four terminals with systematic variation of the biasing conditions and gate voltages, Coulomb oscillation features from different major grains could be identified and from the overall set of measurements the actual locations of these grains on the central cross region of the device could be estimated (e.g. Fig. 3). It appears from these experiments, that major percolation paths between the different leads and across the central region are established.

References:

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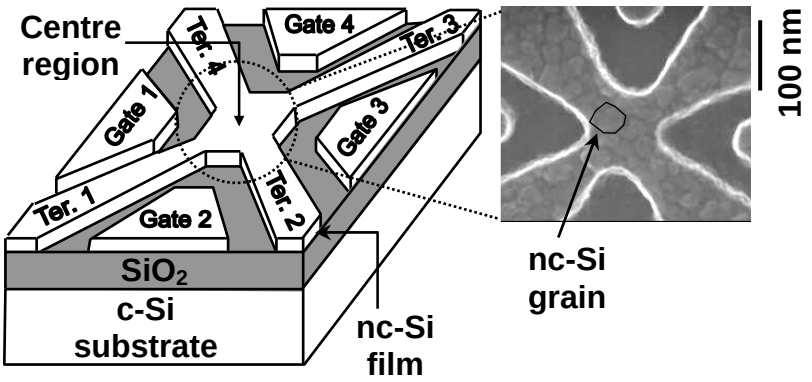

Fig. 1 Schematic of a nanocrystalline silicon (nc-Si) cross transistor. Inset: SEM of a nc-Si cross transistor.

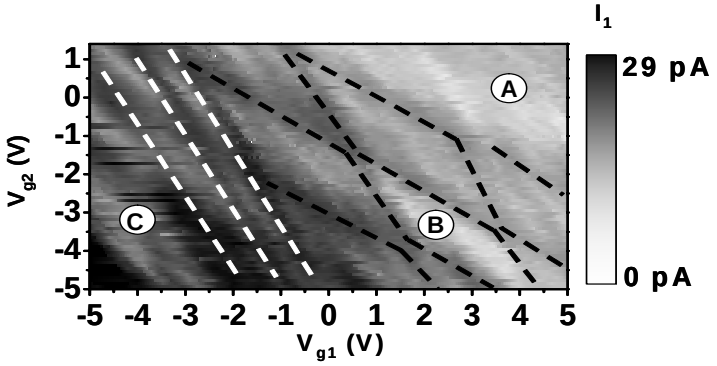

Fig. 2 Current, I_1, at terminal 1 (Ter.1) versus gate voltages, V_{g1} and V_{g2} at V_1 = 3 mV (Ter.1 voltage), $V_{g3} = V_{g4}$ = 0 V and T = 4.2 K. Various coupling effects between the grains are observed in regions A, B, and C.

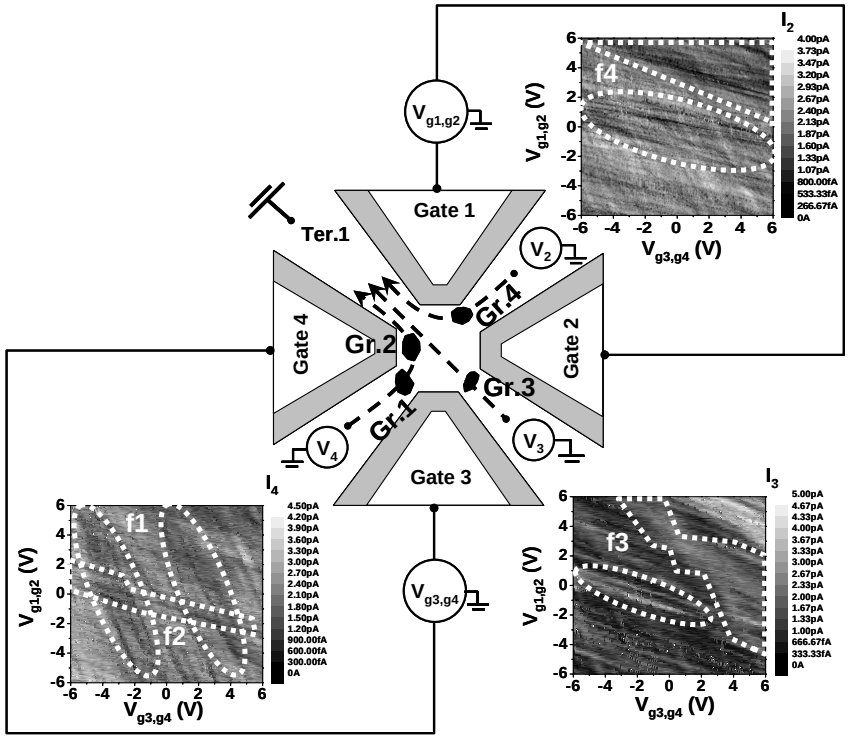

Fig. 3 Set-up, with terminal 1 (Ter.1) grounded, investigating the formation of percolation paths (dashed arrows) in a nc-Si cross transistor. The locations of dominant charging grains (Gr.1 - Gr. 4) are estimated from the Coulomb oscillation features (f1 - f4) in the characteristics of the biased terminals.