Investigation of variable coupling and current percolation paths in nanocrystalline silicon cross transistors

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Nanocrystalline silicon thin films are promising materials for the development of advanced Large Scale Integration compatible quantum-dot and single-electron charging devices [1]. The films consist of nanometer-scale grains of crystalline silicon, separated by amorphous silicon or silicon dioxide grain boundaries up to a few nanometer thick. These films have been used to fabricate single-electron transistor [1] and memory devices [2], where the grains form single-electron charging islands isolated by tunnel barriers formed by the grain boundaries. The grain boundary tunnel barrier isolating the grains is also of great importance, as this determines the extent of the electrostatic and tunnel coupling between different grains. These effects can lead to the nanocrystalline silicon thin film behaving as a system of coupled quantum dots [3, 4].

A novel nanocrystalline silicon 'cross' transistor (Fig. 1, approximately 70 nm × 70 nm × 40 nm), with four side gates and four leads, have been used to study the variation of the electrostatic coupling between the nanocrystalline silicon grains (10 nm to 35 nm in size) as a function of the gate voltages, and to determine the locations of dominant charging grains along the electron current percolation paths. This device allows us to investigate the transition in the conductance mechanism, from conduction through a few grains to conduction through a larger number of grains (Fig. 2). Under an extensive characterization of the currents through the four leads with systematic variation of the biasing conditions and gate voltages, Coulomb oscillation features from different major grains could be identified and from the overall set of measurements the actual locations of these grains on the central cross region of the device could be estimated. It appears from these experiments, that major percolation paths between the different leads and across the central region are established.

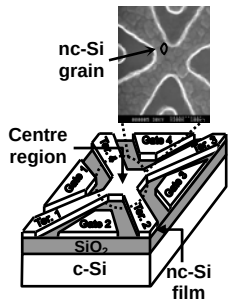

Fig. 1. Schematic of a nanocrystalline silicon (nc-Si) cross transistor. Inset: SEM of a nc-Si cross transistor.

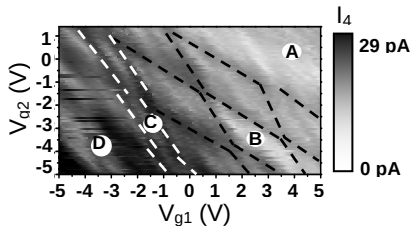

Fig. 2. Current at terminal 4 (Ter.4) versus gate voltages, V_{g1} and V_{g2} at $V_{g3} = V_{g4} = 0$ V and T = 4.2 K. The grains couple differently at regions A, B, C, and D.

References:

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