Bottom-up fabrication of Si nanodot transistors using the nc-Si dots solution

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Introduction

A new approach to fabricate nanometer-scale silicon devices is recently attracting much attention, which combines the conventional top-down silicon processing techniques and the bottom-up assembly of silicon nanodots, whose structures are controlled on the atomic scale. This technique enables to investigate the electronic states and transport properties of strongly-coupled multiple nanodots which will be crucial particularly for quantum information device applications. Various unique properties have been studied in such systems. For example, electrostatic interactions have been investigated for double Si dots [1] and for the two-dimensional Si multidots [2]. Coherent wavefunction coupling and associated quasi-molecular states have also been observed for a tunnel-coupled double Si nanodots [3]. In addition, metal-insulator transition has been investigated for an artificial lattice of self-organized nano-paraticles [4]. In this paper we propose and examine a novel technique of fabricating nanoscale transistors with a Si nanodot cluster as a channel based on the self-assembly of the nanocrystalline Si dots from the solution on the patterned SOI substrates.

Device Structures and fabrication of nano electrodes

Multiple Si nanodots should be placed only between source and drain nanoelectrodes with a gap of a few tens nanometer down to a few nanometer. Figure 1 shows a flow chart of our fabrication process. The electrodes were fabricated by using the heavily-doped silicon on insulator (SOI) with thickness of about 50nm and the buried oxide (BOX) thickness of 200nm. This structure gives a good areal contrast of hydrophobic (Si) and hydrophilic (SiO_2) surfaces and works as a template for the following nc-Si dots assembly process. First a 50nm-thick SOI film, whose thickness was controlled by thermal oxidation at 1100℃ for 50min, was doped heavily by ion implantation (*n*-type, phosphorous, doping concentration $\sim 1 \times 10^{20} cm^{-3}$). The nano electrodes were then patterned with electron beam lithography with ZEP520 positive resist. Electron cyclotron resonance reactive ion etching (ECR-RIE) was used to transfer the resist pattern onto the SOI layer, and CF_4 was used as an etching gas. Figures 2 and 3 show SEM images of two-terminal and four-terminal electrode structures, respectively. We were able to obtain the two-terminal electrodes with a minimum interelectrode gap of 7nm and the four-electrodes with that of 15nm.

Fabrication of channel region

Nanocrystalline silicon (nc-Si) dots are fabricated by using the VHF plasma CVD. Diameter of the nc-Si dots are controlled well to be 8nm±1nm. However, the nc-Si dots are deposited randomly on the substrate. Therefore we adopted the nc-Si dot solution technique for forming the channel region. We used a drop and evaporation technique [5] to assemble the nc-Si dots from the dispersion solution by using the lateral capillary meniscus force, which works at the point where the three phases of the liquid, air and nc-Si dot meet. Figure 4 shows the nc-Si dots assembled on the SOI substrate with a patterned nanogap of about 35 nm. We observed that nc-Si dots remained only in the SiO_2 regions and were assembled near the nano gap, resulting in a nc-Si dot channel between the electrodes. This trend was observed in common over the large area. This method may be useful to fabricate the nc-Si dot channel of nanoscale transistors, and we believe that it is possible to form a channel with few nc-Si dots or even a single dot by reducing the density of nc-Si and optimizing evaporation conditions. The electrical properties of the fabricated devices will also be discussed.

Summary

The nano electrodes with the interelectrode gap of 7nm for the two-terminal and 15nm for the four-terminal were fabricated successfully. We examined the assembly of the nc-Si dots on the patterned electrodes with a nanoscale gap and succeeded in fabricating the nc-Si dots cluster bridging between the electrodes.

Acknowledgment

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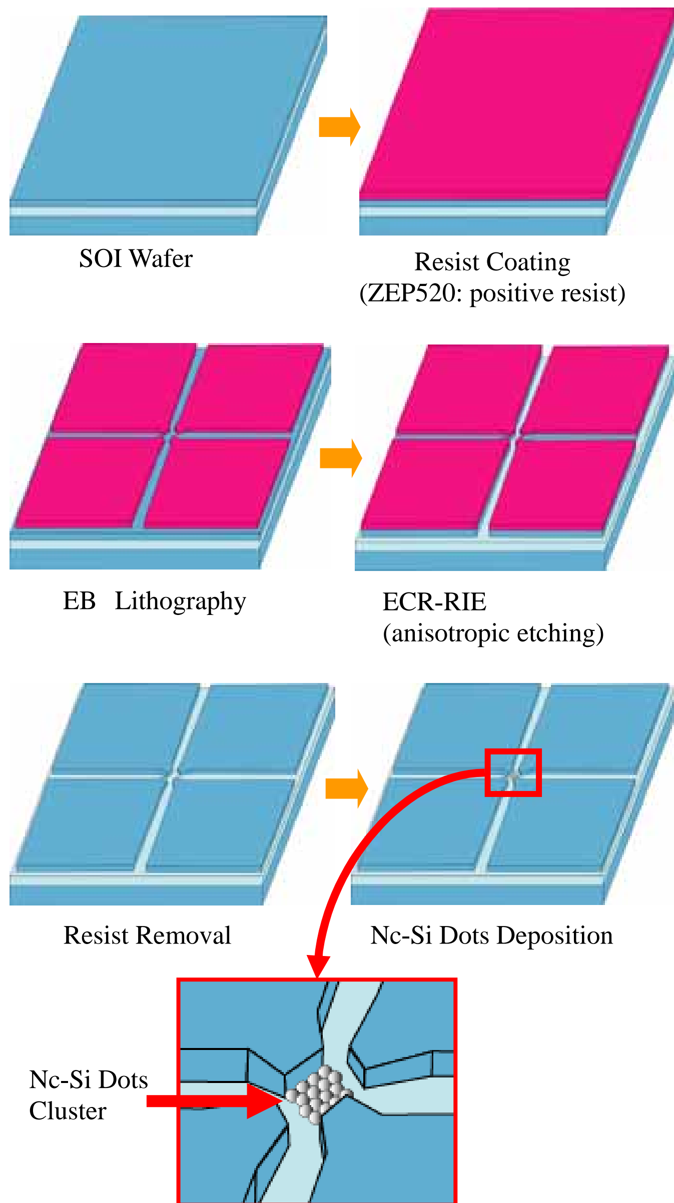

Fig. 1: A schematic illustration of device fabrication process. Source, Drain, and Gate are heavily doped SOI and the channel region is formed by multiple nc-Si dots.

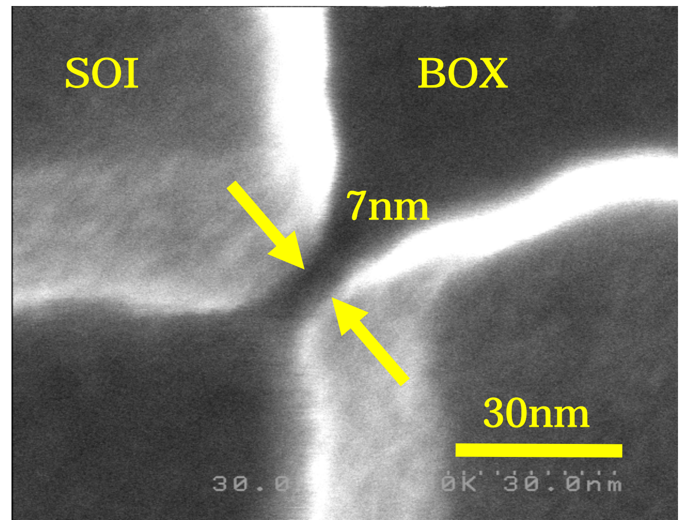

Fig. 2: SEM image of a two terminal nano electrode which has a minimum interelectrode gap of about 7nm.

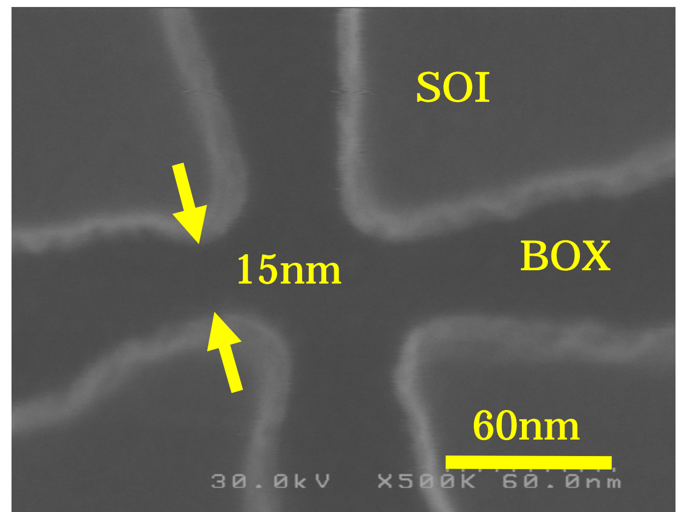

Fig. 3: SEM image of a four terminal nano electrode which has a minimum interelectrode gap of about 15nm.

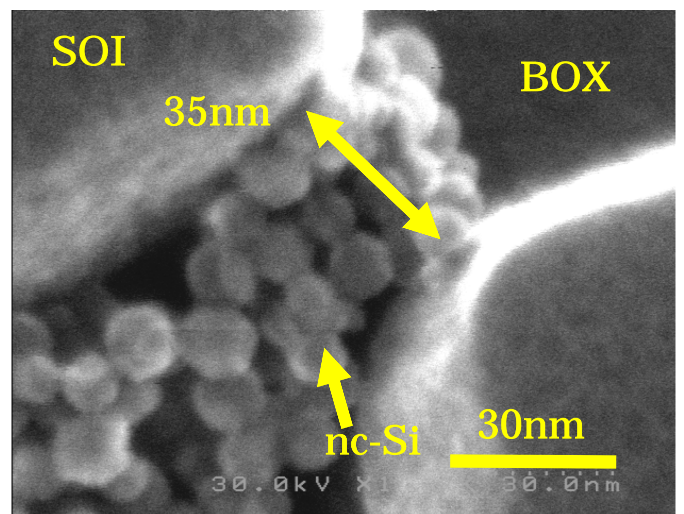

Fig. 4: SEM image of the channel region which is fabricated using nc-Si dots solution.