The Dependence of Deca-nanometer Poly-Si Thin Film Transistor Output Characteristics on the Grain Boundary Location

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I. Introduction

Poly-Silicon thin-film transistors (TFTs) have been studied extensively in recent years for their application in flat panel active matrix liquid crystal displays(AMLCD). It has been suggested that the TFTs could be used for an integrated driving circuit of the display. To facilitate the required high performance, much effort has been made to increase both the grain size and therefore the mobility in poly-Si films [1].

In scaling the channel of the device down to the decananometre regime - a length and width comparable to the poly-Si grain size - it is important to understand the effects of discrete GBs on conduction [2] [3]. Furthermore in a device of these dimensions we can no longer ignore where the grain boundaries are located within the channel.

II. Summary of Results and Discussion

We investigated the special situation where only a single GB perpendicular to the channel is present in the device. A situation likely to be found when the grain size is comparable to channel length [4]. Under such circumstances it is natural to expect some variation of the device characteristics with grain boundary position. Recent studies have shown that the threshold voltage of TFTs is strongly influenced by the grain boundary position [5]. We aimed to investigate if there was an equally strong influence on the output characteristics of TFTs.

A commercially available 2D device simulator, ATLAS, was used in our simulations. A high density of trap states are localised at the grain boundary region. It was assumed that the the trap states distributed in the forbidden energy gap were comprised of both donor and acceptor type traps [6] as shown in Fig 1.

The position of the GB was varied in a TFT with a channel length of 50nm (Fig 2). We investigated its effect when located 10nm from the source edge (device A), 10nm from the drain edge (device B) and finally when there was no GB present in the channel(device C).

Our simulation results shown in Fig 3 displayed a strong dependence on the GB position. The resulting output characteristics showed that device B had very poor characteristics with no current saturation, whereas, device A had very good saturation but a low drain current.

With device C we observed reasonable current saturation. However the saturation was not as good as for device A, however the drain current was larger.

The poor characteristics of the device with a GB close to the drain can be explained by looking a the conduction band diagram of the device in the saturation region (Fig 4). It was found that if the GB is located too close to the drain there is a reduction in the effective channel length of the device resulting in increased short channel effects and poor current saturation. However if the GB is located near the source edge there is no reduction in effective channel length and instead the GB acts as a very large source resistance. Therefore such a device shows improved saturation at the cost of a decrease in drive current.

Fig 5. shows the drain conductance in the "saturation region" as a function of GB position. It was found that the drain conductance increases rapidly as the GB is moved closer to the drain edge.

III. Conclusions

Our studies show that control of the position of the Grain Boundary in the channel is critical for good device performance in TFTs with decananometer channel lengths. Therefore design and control of the position of the grain boundaries in TFTs is desirable for optimal device performance.

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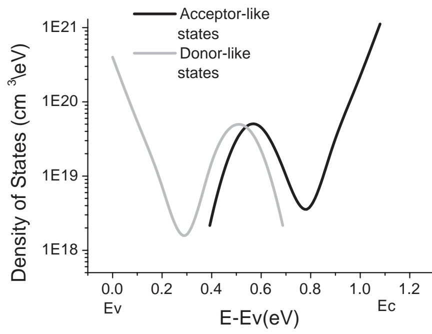

Fig 1. Density of states for the carrier traps in the forbidden energy gap of the Poly-Si grain boundary regions that was used the simulations

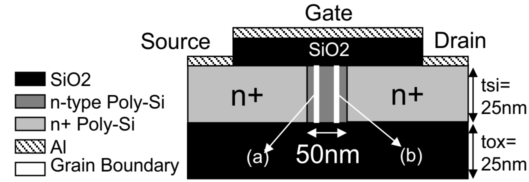

Fig 2. Device Structure and relative position of the GB (a) 10nm from source. (b) 10nm from drain

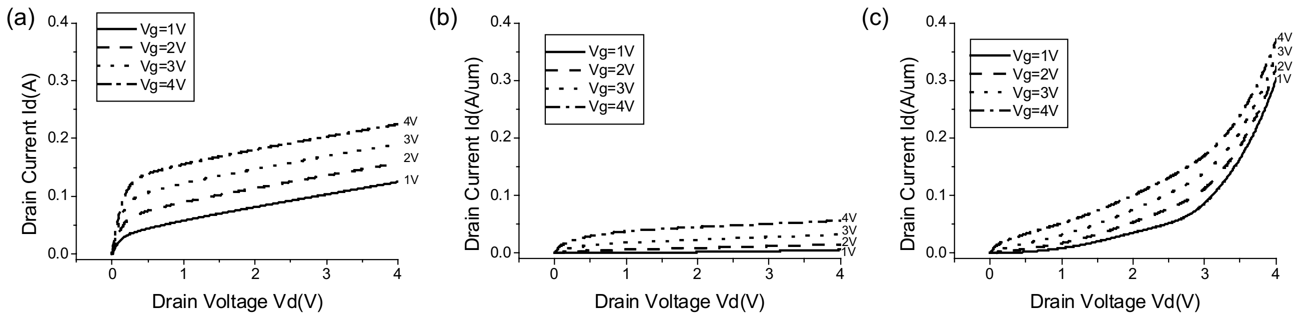

Fig 3. Id-Vd characteristics for a 50nm TFT with (a) device with no GB in the channel (b) device with GB 10nm from the source edge (c) device with GB 10nm from the drain edge

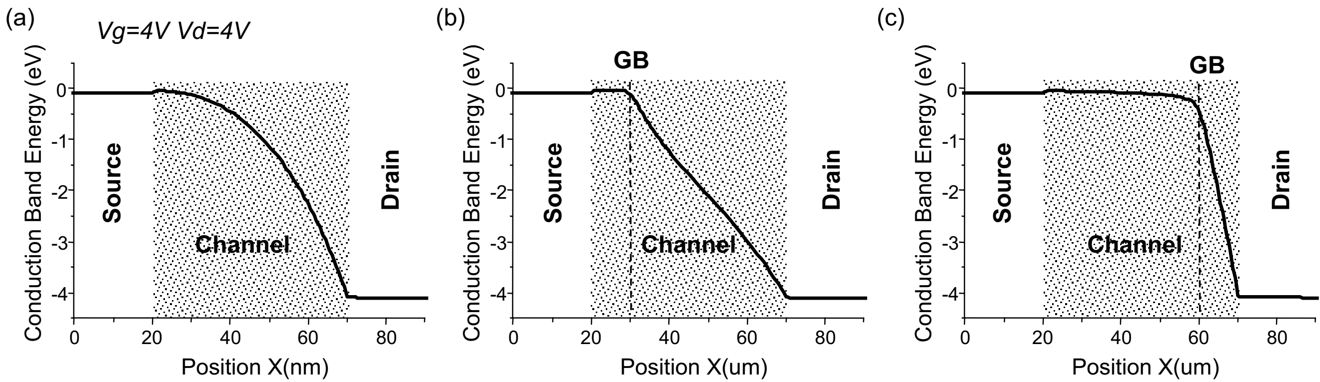

Fig 4. Conduction band potential close to the interface under the bias condition Vd=Vg=4V for a device with (a) no GB (b) GB 10nm from the source (c) device with GB 10nm from the drain

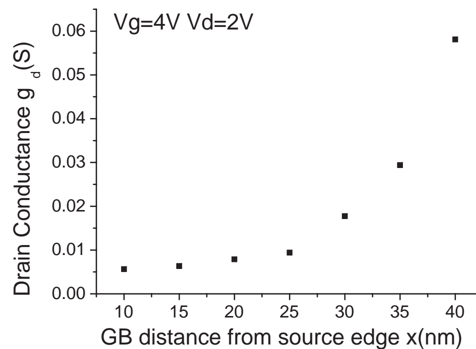

Fig 5. Drain conductance at Vg=4V and Vd=2V as a function of the GB position relative to the source edge