

Improved device characteristics for deca-nanometre scale TFTs with a single GB in the channel

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A simulation model for deep trap states at grain boundaries in Poly-Si TFTs has been developed. The model was used for simulation of single GB TFT devices with sub micron channel lengths. The transport physics have been clarified and it was found that in short channel devices ($L_{eff} < 100nm$) the single GB TFT shows improved subthreshold behaviour and OFF current compared to its SOI equivalent.