Grain Boundary Effects on Subthreshold Behaviour in Single Grain Boundary nano-TFTs

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WE have found that for device simulations of aggressively scaled poly-silicon thin film transistors the presence of a GB at the centre of the TFT channel aids in both suppression of the off current and improving the subthreshold slope.

Poly-silicon thin-film transistors (TFTs) have been studied extensively in recent years for their application in flat panel active matrix displays. When poly-Si TFTs are used in AMLCD applications the minimum feature size is typically very large $>> 10\mu m$ and therefore a large number of GBs are present in the channel. Conventionally, the effect of the GBs is considered to reduce the electron mobility below the bulk-single crystal value. In such an analysis the discrete properties of individual GBs are not considered. However for applications in 3D VLSI the device must be scaled to much smaller dimensions [1]. In scaling the channel of the device down to the nanometre regime - a length and width comparable to the poly-Si grain size -, it is increasingly important to understand the discrete effects of a grain boundary (GB) on conduction [2].

Previously, the approach taken to improve poly-Si TFT characteristics has been to reduce the number of defect states at the GBs or reduce the number of GBs in the channel. [3] We aimed to find if there was a situation where through clever device design, the GBs could enhance TFT characteristics.

A Poly-Silicon TFT with a single grain boundary (GB) present in the channel is simulated using 2D numerical simulation (Fig. 1) which includes a model of deep trap states at GBs.[4]. Our model was verified by modelling a known experimental result (Fig 2.) for a TFT with 2 perpindicular GBs in the channel region and good agreement was found. [5]

The conduction mechanism in the TFT was clarified. The turn on characteristics of the device are controlled primarily by Gate Induced Grain Barrier Lowering (GIGBL) as opposed to modulation of carriers in the channel by the gate voltage.

In the subthreshold regime our simulations indicate that the grain boundary suppresses the large off currents found in short channel devices(Fig 3). In 50nm SOI MOSFET short channel effects have an unacceptably detrimental effect on subthreshold slope and off-current[6], the GB in the TFT channel alleviates these problems(Fig 4).

References

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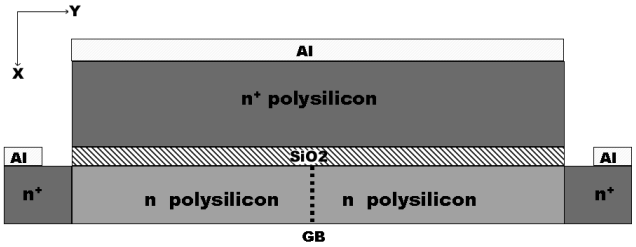

Fig 1. The 2D device structure used for the TFT simulation

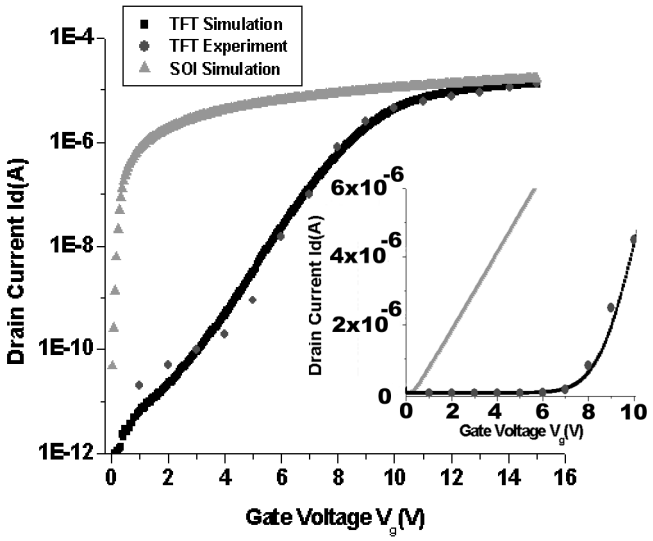

Fig 2. Comparison between simulated and experimental linear Id-Vg characteristics for a p-channel inversion mode TFT with two lateral GBs in the channel region.

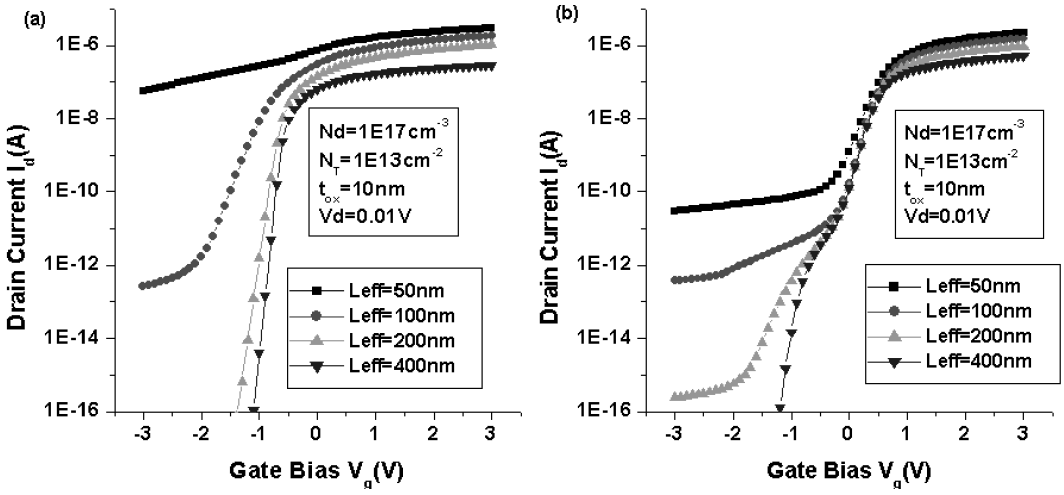

Fig 3. (a) SOI MOSFET (b) single-GB TFT - The single GB TFT shows better subthreshold behaviour when the channel length is scaled below $0.1\mu m$ Turn on is by GIGBL and additional current suppression in the off regime is provided by the GB potential barrier.

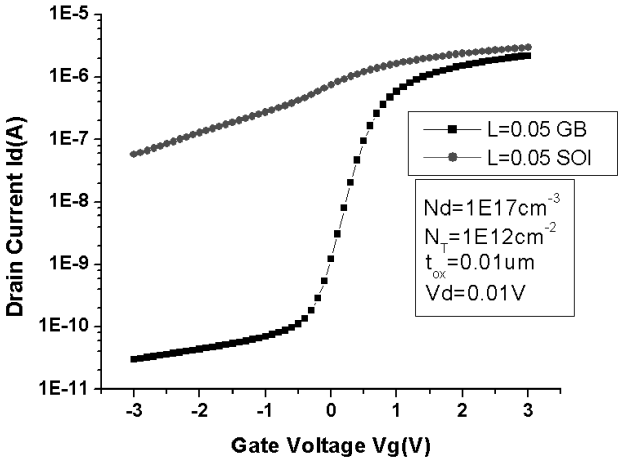

Fig 4. Here the channel length is scaled down to 50nm. By direct comparison of the Id-Vg characteristics of a single GB TFT and a same geometry SOI device it is easy to see that the GB improves the subthreshold behaviour.

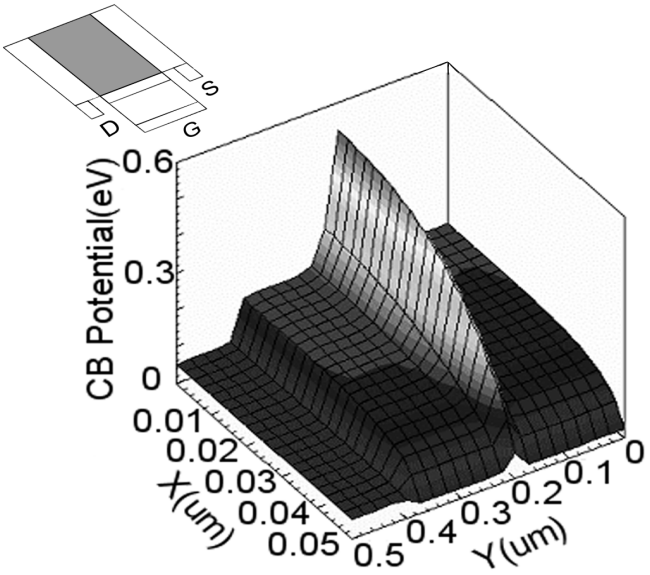

Fig 5. A plot of the conduction band potential over the channel indicated by the shaded area on the device diagram. At Vd=0.01V and Vg=1V the potential barrier near the interface in lowered significantly (GIGBL).