NANOSILICON FOR SINGLE-ELECTRON DEVICES

H. Mizuta[1,4], Y. Furuta[1,4], T. Kamiya[2,4], Y. T. Tan[3,4], Z.A.K. Durrani[3,4], K. Nakazato[1,4] and H. Ahmed[3,4]

[1]Hitachi Cambridge Laboratory, Hitachi Europe Ltd., Madingley Road, Cambridge CB3 0HE UK
[2]Materials and Structures Laboratory, Tokyo Institute of Technology, 4259 Nagatsuka, Midori-ku, Yokohama 226-8503, Japan
[3]Microelectronics Research Centre, University of Cambridge, Madingley Road, Cambridge CB3 0HE, UK
[4]CREST JST (Japan Science and Technology), Shibuya TK Bldg., 3-13-11 Shibuya, Tokyo 150-0002, Japan

This paper gives an overview of our recent work investigating nano/polycrystalline silicon nanostructures for single-electron device applications. Nano/poly-Si nanowires have been used as a key building block for nanoscale memory and logic devices based on the Coulomb blockade phenomenon by utilising individual silicon grains and grain boundaries as an electron island and a tunnel junction. However, the microscopic properties of the grain boundaries as a tunnel barrier have not been made clear, and there is no guideline to optimise the grains and grain boundaries in terms of high temperature Coulomb blockade operation.

We first provide a short summary on the research of silicon-based single-electron devices from the last decade. Various single-electron transistor structures are compared in terms of control of electron islands and tunnel barriers. We then investigate the single-electron charging phenomena in nano/polycrystalline silicon nanostructures. A novel point-contact transistor (Fig. 1) is introduced, which features an extremely short and narrow nano/poly-Si nanowire as the transistor's channel [1]. This structure is suitable for studying how a grain smaller than 10 nm in size and a discrete grain boundary work as a charging island and a tunnel barrier, respectively. The relationships between structural and electrical parameters of grains/grain-boundaries and the resulting Coulomb blockade characteristics (Fig. 2) [2] for the point contact transistors are investigated by applying various passivation processes such as multiple step oxidation [3][4]. Finally, a possibility of controlling and optimising grain and grain-boundary properties is discussed for improving the Coulomb blockade characteristics and realizing nano/poly-Si single-electron transistors operating at room temperature [5].

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[1] mizuta@phy.cam.ac.uk

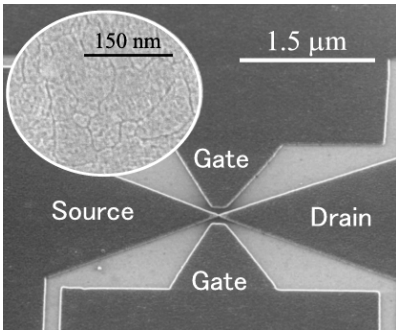

Fig. 1 *A SEM image of an as-prepared point contact transistor with a channel 30-nm-wide and 30-nm-long. The inset figure shows the grain structure of Secco-etched poly-Si film. Lateral dimension of grains in the film ranges from 20 nm to 150 nm.*

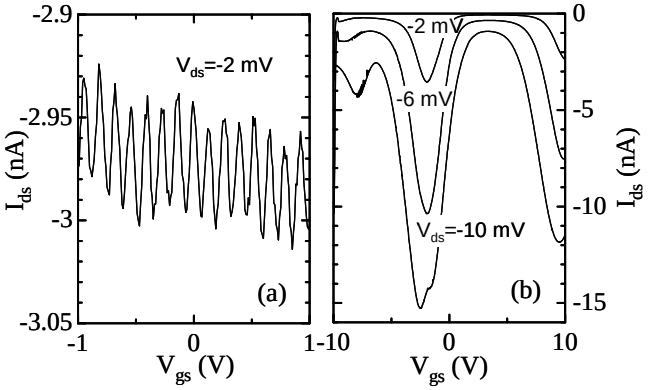

Fig. 2 *Two types of I_{ds}-V_{gs} characteristics observed for point-contact transistors oxidized at 1000 ^{o}C for 15 minutes. Difference in the Coulomb oscillation period and current peak-to-valley ratio are attributed to different size of charging island and tunnel barrier properties.*