Effects of oxidation and annealing temperature on grain boundary properties in polycrystalline silicon probed using nanometer-scale point-contact devices

Toshio Kamiya[1,3,4], Yoshikazu Furuta[2,3], Yong-Tsong Tan[1,3], Z. A. K. Durrani[1,3], Hiroshi Mizuta[2,3] and H. Ahmed[1,3]

[1]Microelectronics Research Centre, University of Cambridge, Madingley Road, Cambridge CB3 0HE, United Kingdom

[2]Hitachi-Cambridge Laboratory, Cavendish Laboratory, Madingley Road, Cambridge CB3 0HE, United Kingdom

[3]CREST, JST, 3-13-11 Shibuya, Tokyo 150-0002, Japan

[4]Materials and Structures Laboratory, Tokyo Institute of Technology, 4259 Nagatsuta, Yokohama 226-8503, Japan

Carrier transport in polycrystalline silicon (poly-Si) is affected significantly by electronic properties of grain boundaries (GBs). As future nanometre-scale devices, such as single-electron transistors (SETs), will have only a few GBs in the active region, the control and characterization of individual GBs will be vital to obtain reliable and reproducible device operation.

We have characterized individual GBs in poly-Si using nanometer-scale devices.[1,2] In this work, we focus on the effects of oxidation and annealing temperature on the electrical characteristics of GBs. We have fabricated 30-nm-wide point-contact devices in a 50-nm-thick highly-doped n-type poly-Si film. The channel length was varied from 20 nm to 80 nm. These devices were subjected to oxidation in dry O_2 gas at 650^{o}C - 1000^{o}C for 1 hr. Some devices were followed by annealing in Ar ambient at 1000^{o}C for 15min after the oxidation. We have observed that oxidation at 650^{o}C - 750^{o}C oxidises the grain boundaries selectively, and that subsequent annealing increases the associated potential barrier height and tunnel resistance. These are explained by structural changes in the Si-O network at the grain boundaries and the competition between surface oxygen diffusion and oxidation from the GBs into the crystalline grains.

e-mail: tkamiya@rlem.titech.ac.jp
The mail address is
Toshio Kamiya
Materials and Structures Laboratory, Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama 226-8503, Japan

Reference

[1] Y. Furuta, H. Mizuta, K. Nakazato, Y.T. Tan, T. Kamiya, Z.A.K. Durrani, H. Ahmed and K. Taniguchi. Jpn. J. Appl. Phys. **40** (2001) L615-L617.

[2] Y. Furuta, H. Mizuta, K. Nakazato, T. Kamiya, Y.T. Tan, Z.A.K. Durrani and K. Taniguchi, Jpn. J. Appl. Phys. **41** (2002) 2675-2678.