Single-electron charging phenomena in nano/polycrystalline silicon point-contact transistors

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This paper gives a review of our recent study done in the area of Coulomb blockade (CB) devices based on polycrystalline silicon nanostructrues. Poly-Si nanowires (NWs) have been used as a key building block for CB memory and logic devices by utilising individual silicon grains and grain boundaries (GBs) as an electron island and a tunnel junction. However, the microscopic properties of the GBs as a tunnel barrier have not been made clear, and there is no guideline to optimise the GBs in terms of high temperature CB operation. To clarify these we adopt poly-Si point contact transistors (PC-Trs) where both length and width of the poly-Si NW channel are designed to be from 30 nm to 50 nm, which are as small as the size of individual grains (Fig. 1). PC-Trs therefore contain either zero or only a few GBs at most in the channel and enable us to study electron transport via a few GBs and associated charging phenomena. We first study the properties of GBs in the as-prepared PC-Trs [1] and then show how parameters of GBs as a tunnel barrier vary with changing process conditions (Fig. 2) [2]. We finally discuss a possibility of optimising the GBs for increasing the operating temperature of the poly-Si CB devices towards room temperature [3].

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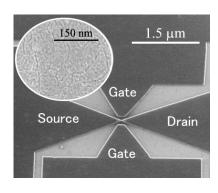


Fig. 1 SEM image of an as-prepared PC-Tr with a channel 30-nm-wide and 30-nm-long. The inset figure shows the grain structure of Secco-etched poly-Si film.

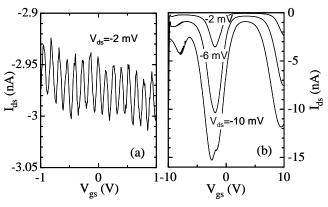


Fig. 2 Two types of I_{ds} - V_{gs} characteristics observed for PC-Trs oxidized at 1000 °C for 15 minutes. Difference in CB oscillation period and current P/V ratio are attributed to different size of charging island and GB tunnel barrier properties.