Improved Sub-threshold Slope in RF Vertical MOSFETS using a Frame Gate Architecture

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Abstract-**We report a CMOS-compatible vertical MOSFET, which incorporates a frame gate architecture suitable for application in RF circuits. Fabricated surround gate vertical MOSFETs with the frame gate architecture show no degradation of short channel effects when the channel length is scaled, while control devices show significantly degraded sub-threshold slope and DIBL. The frame gate vertical MOSFETs show near ideal sub-threshold slopes of 70-80mV/decade and DIBL of 30-35mV/V in a 100 nm gate length nMOS device. In contrast, the control vertical MOSFETs without the frame gate exhibit sub-threshold slopes of 110 to 140 mV/decade and DIBL of 100 to 280 mV/V. This improved sub-threshold slope is explained by the elimination of etch damage during gate etch.**

1. INTRODUCTION

Thin pillar, fully depleted, double gate vertical MOSFETs are being researched as candidates for end-of-roadmap CMOS technology because they have advantages such as improved short channel effects and improved drive current [1-2]. However, these devices require advanced lithographic techniques and/or complicated processing to define the ultra thin channel. Thick pillar, surround gate, vertical MOSFETs are also of interest because they offer lithography-independent channel length scaling, decoupling of the gate length from the packing density and an improved current drive per unit silicon area compared with conventional lateral CMOS [3-4]. This approach is particularly attractive for RF applications, since it enables a short channel vertical RF transistor to be integrated in a mature CMOS technology. The main disadvantages of vertical MOSFETs for this application are high overlap capacitance and susceptibility to dry etch damage. We have previously reported a CMOS compatible Fillet Local Oxidation (FILOX) Process [5], which uses a nitride spacer on the pillar sidewall and local oxidation to reduce the overlap capacitance at the top and bottom of the pillar. In this paper, we propose a frame gate architecture, which is suitable for RF applications, compatible with the FILOX process and immune to dry etch damage. While conventional FILOX transistors exhibit sub-threshold slopes of 110 to 140 mV/decade and DIBL of 100 to 280 mV/V for a channel length of 100 nm, the frame gate transistors are found to have significantly improved immunity to short channel effects, with near ideal sub-threshold slopes of 70 to 80 mV/decade, and DIBL of 30 to 35 mV/V.

2. DEVICE FABRICATION

Boron-doped (0.75-1.25 Ω.cm) (100) wafers were taken as the starting material and a p-type body was formed by boron implantation (1.2×10^{14}/cm^2, 75 keV, 7 degree tilt) and high temperature drive-in. The FILOX (Fillet Local Oxidation) process [5] used a 65nm wide nitride fillet on the pillar sidewalls and a 60 nm oxide layer was thermally grown at 1100°C. The source/drain electrodes were implanted (Arsenic, 6×10^{15}/cm^2, 100 keV, 0 degree tilt) and the nitride fillets and pad oxide were subsequently removed. A 2.6nm gate oxide was then grown at 700°C and a 150nm in-situ doped (P, 1×10^{20}/cm^3) polysilicon gate was deposited and patterned by dry etch. An RTA at 1100°C for 10 sec was performed for dopant activation. Fig.1 compares the fabricated FILOX transistor with a conventional vertical MOSFET. As can be seen, the FILOX oxide (Fig. 1(B)) provides a significant reduction of the gate overlap capacitance.

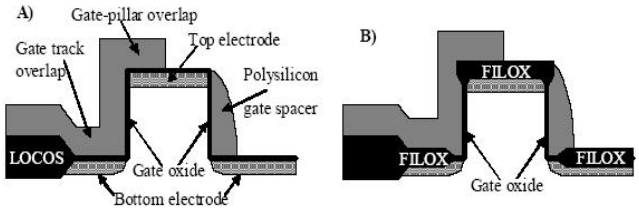

Fig.1: Schematic cross sections of a conventional vertical MOSFET (A) and a FILOX vertical MOSFET (B).

3. FRAME GATE LAYOUT

Fig.2 illustrates the different layouts used for the fabricated devices. Fig. 2 (a) shows the conventional surround gate vertical MOSFET, where a polysilicon spacer surrounds the pillar sidewall and a single polysilicon track is used to contact the polysilicon spacer. Fig. 2 (b) shows a similar double gate contact device where two gate tracks are used to contact the polysilicon spacer at either side of the pillar. Fig. 2 (c) shows the frame gate architecture, where a thin frame of polysilicon surrounds the pillar to aid the circulation of RF currents. In this layout, the polysilicon gate is contacted on top of the pillar. Fig. 2 (d) shows a control device for the frame gate structure where a contact to the gate polysilicon is provided on top of the pillar, but no polysilicon frame is present. Fig.3 shows the corresponding plan-view optical microscope images of the fabricated transistors.

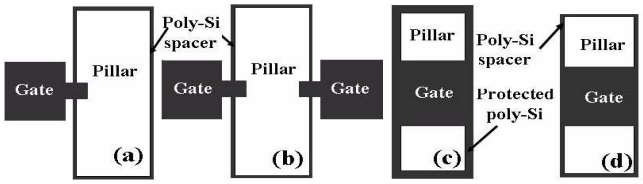

Fig. 2: Mask layouts showing the different types of fabricated device, a) Single gate contact b) double gate contact c) frame-gate device and d) control device

4. PROCESS CHARACTERISATION

Fig. 4 shows a SEM micrograph of a pillar just after FILOX oxidation. The original pillar height before oxidation was derived from a profilometer measurement and its height of

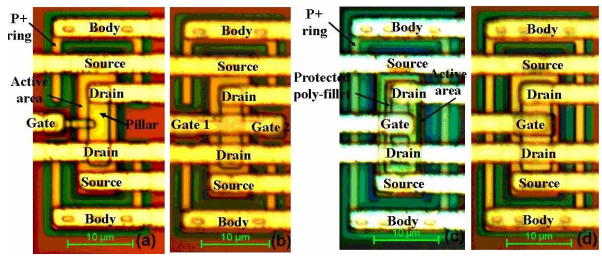

Fig. 3: Optical microscope images of devices with a) single gate contact b) double gate contact c) frame-gate and d) control layout.

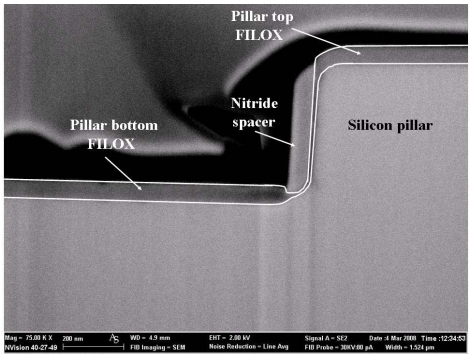

Fig. 4: SEM cross-section of the FILOX process directly after the FILOX oxidation. The edge of the FILOX oxide layer has been highlighted for clarity.

500 nm can be estimated from the SEM image. The figure clearly shows the 65 nm nitride spacer and the presence of the FILOX oxide at the top and bottom of the pillar. The FILOX oxide is 60 nm, in agreement with expectations. It can be seen that the nitride spacer is effective in protecting the Si channel very well against oxide encroachment both at the top and bottom of the pillar.

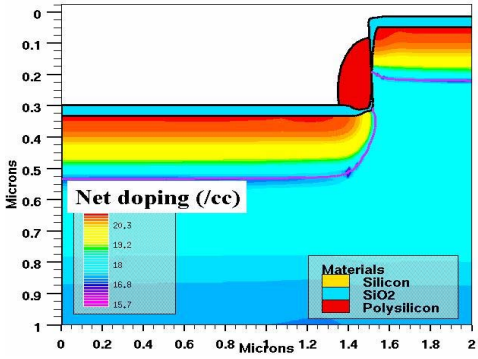

Fig. 5: Simulated source and drain doping profiles at the completion of the process.

The channel is difficult to electrically measure in vertical MOSFETs and hence we have used a combination of SEM measurements of the pillar heights and process simulations of the source and drain junction depths to extract values of channel length for the four different pillar heights fabricated. The simulations were performed using the Silvaco ATHENA software. To accurately model dopant diffusion and activation, a fully coupled simulation was performed, with cluster damage and high concentration diffusion models included. Fig. 5 shows the ATHENA simulation result for a 300 nm pillar. Junction depths of 180 and 190 nm are obtained for the pillar top and bottom respectively. This gives a channel length of around 100nm for a 300 nm pillar.

As profilometer measurements showed pillar heights of 300, 350, 400 and 450 nm, we therefore conclude that the corresponding channel lengths were 100, 150, 200 and 250 nm respectively.

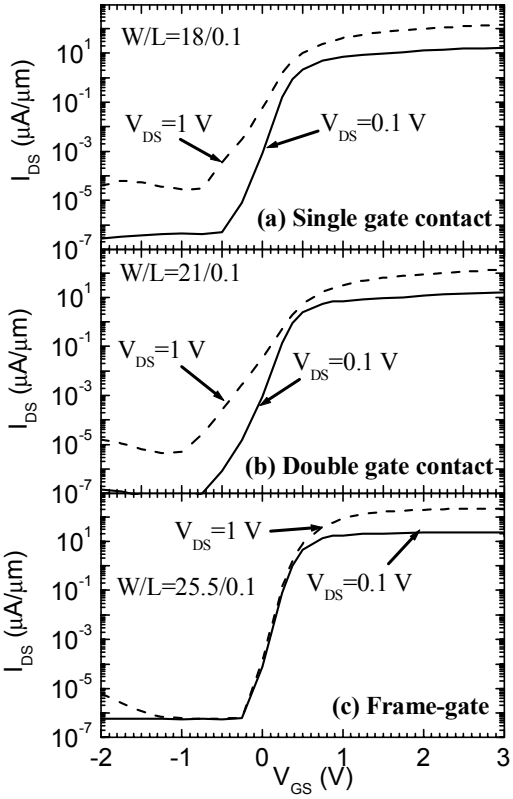

Fig. 6: Transfer characteristics of surround gate vertical NMOS devices with a channel length 100 nm; a) Single gate contact b) double gate contact and c) frame-gate structure.

5. ELECTRICAL RESULTS

Fig. 6 shows transfer characteristics of surround gate vertical MOSFETs with single and double gate contacts and of a frame gate device. All devices have the same channel length of 100 nm. For the single gate contact device in Fig. 6 (a) a sub-threshold slope of 115 mV/decade is observed. The drain induced barrier lowering (DIBL) is estimated using the constant current threshold method. The shift in I_{DS}-V_{GS} curves has been calculated for I_{DS} of 1 μA and found to be 220mV/V. A similar behaviour is observed for the double gate contact device in Fig. 6(b), which has a sub-threshold slope of 115 mV/decade and a DIBL of 176mV/V. In contrast, for the frame-gate device in Fig. 6(c) a significantly improved characteristic is observed with a sub-threshold slope of 78 mV/decade and almost no DIBL; *i.e.* 35 mV/V.

Fig. 7 shows the output characteristics of surround gate vertical MOSFETs with single and double gate contacts and of a frame gate device. The highest value of drive current is obtained for the frame gate transistor, and the lowest for the transistor with a single gate contact. The device with a double gate contact has an intermediate value of drive current.

Fig. 8 shows the sub-threshold characteristics of a 100nm control device, which has a gate contact on top of the pillar, but no frame gate (see figure 3(d)). This device exhibits a sub-threshold slope of 110 mV/decade and a DIBL of 100

mV/V, which is similar to the behaviour observed for the devices with single and double gate contacts. This result demonstrates that the improved performance of the frame gate transistor in fig.6(c) is due to the presence of the polysilicon frame.

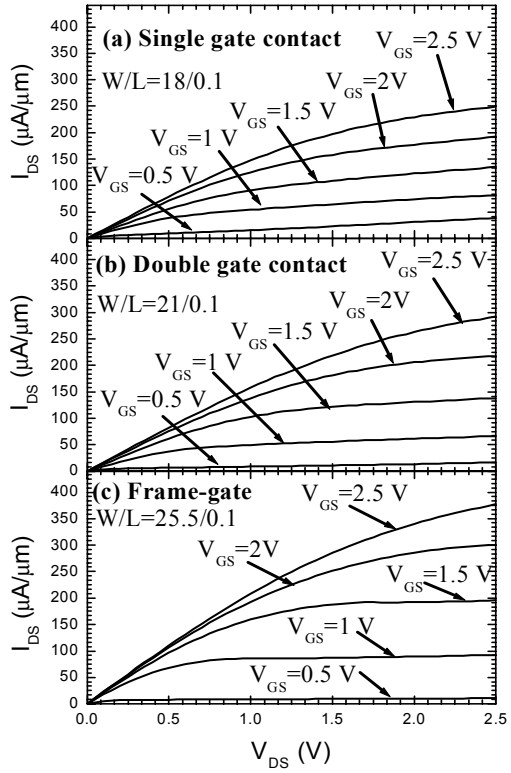

Fig. 7: Output characteristics of surround gate vertical NMOS devices for an approximate channel length 100 nm; a) Single gate contact b) double gate contact and c) frame-gate structure.

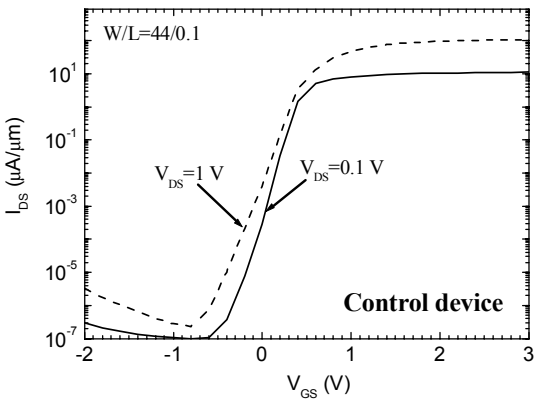

Fig. 8: Transfer characteristics of a control surround gate vertical NMOSFET with a channel length 100 nm (see figure 3(d)).

Fig.9 shows the effect of channel width on the sub-threshold slope and DIBL for transistors with single and double gate contacts, for frame-gate transistors and for control transistors. It can be seen from Fig. 9(a) that the frame gate transistor has significantly better sub-threshold slope (70 to 80 mV/decade) than any of the other transistors (110 to 140 mV/decade) for all channel widths. A similar trend can also be observed in Fig. 9(b) for the DIBL. The frame-gate transistors have values of DIBL in the range 30 to 35 mV/V, whereas the other transistors have values in the range 100 to 280 mV/V.

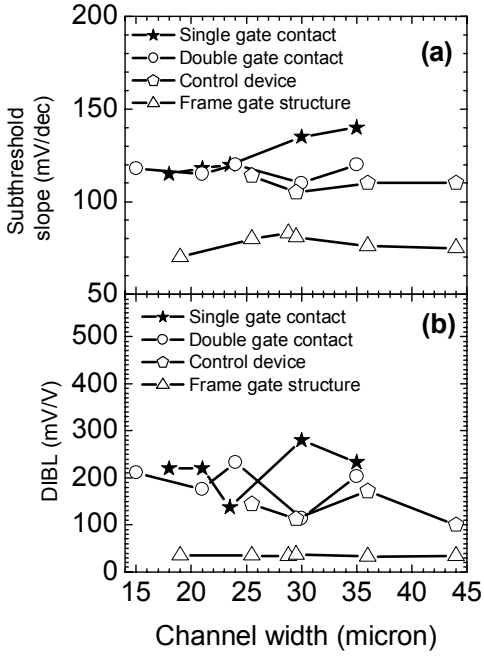

Fig. 9: a) Sub-threshold slope and b) DIBL as a function of channel width for different types of surround gate vertical NMOS device. The transistors have a channel length of 100 nm.

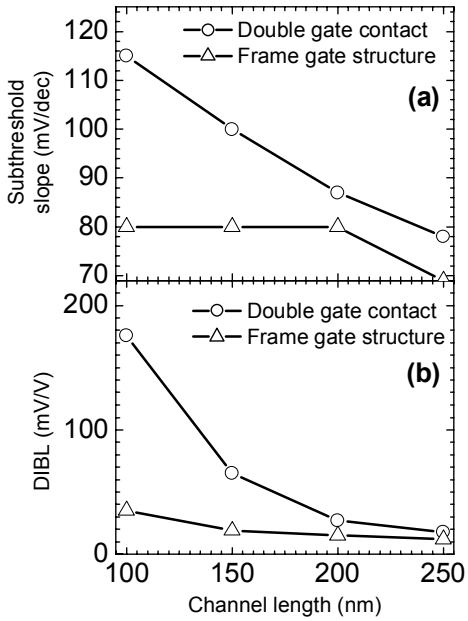

Fig.10: Sub-threshold slope and DIBL as a function of channel length for different types of surround gate vertical NMOS device.

6. SHORT CHANNEL EFFECTS

Fig.10 shows the effect of channel length on the sub-threshold slope and DIBL for transistors with a double gate contact and a frame-gate structure. Fig. 10 (a) shows that for the transistor with a double gate, the sub-threshold slope degrades from 78 to 115 mV/decade as the channel length decreases from 250 to 100 nm. In contrast, for the frame gate transistor, the sub-threshold slope only varies from 70 to 80 mV/decade. A similar trend is observed in the DIBL results, with the frame gate transistor showing a much smaller degradation than the transistor with a double gate contact. These results show that the frame gate device is more immune to short channel effects than the transistor with a double gate contact.

7. DISCUSSION

Table: I compares the frame-gate vertical MOSFET with other vertical MOSFETs reported in the literature. The data has been taken from [3] and updated with recent results on vertical MOSFETs. To ensure a meaningful comparison, fully depleted, thin pillar vertical MOSFETs are excluded from the table, because improved short channel effects would be expected from these devices due to the action of the dual or surround gate. I_{on} has been calculated for $V_{DS}=V_{DD}$ and for a 1V gate-overdrive, whereas I_{off} has been estimated for $V_{GS}=0V$ and $V_{DS}=V_{DD}$ except devices from ref. [4, 8, 9] where due to unavailability of data I_{off} has been estimated for $V_{GS}=0V$ and $V_{DS}=V_{DD}\approx 1V$. As can be seen, the frame gate architecture delivers state of the art values of sub-threshold slope and DIBL in spite of the lower value of body doping than most of the devices. The sub-threshold slope and DIBL approach almost ideal values, which have previously only been reported for thin pillar, fully depleted vertical MOSFETs [1] [2].

Table I: Comparison of the frame-gate device with reported vertical MOSFETs from the literature

Parameters	Schulz et al [3]	Schulz et al [3]	VRG [6]	VRG [6]	Mori et al [7]	Gili et al [8]]	Moers et al [9]	Jayanaraya net al [4]	Frame-gate
L (nm)	100	50	100	50	100	70	50	50	100
t_{ox}(nm)	3	3	2.8	2.8	7	3	6.6	4	2.6
N_A (10^{17}/cc)	20	70	35	35	20	30	2	25	10
V_{DD}(V)	1.5	1.5	1.5	1.5	1.5	1	-1.5	-1.5	1.5
I_{on} (μA/μm)	240	80	140	100	160	0.2-19	270	2.25	160
I_{off} (A/μm)	5×10^{-12}	2×10^{-8}	1×10^{-12}	3×10^{-11}	$<10^{-13}$	6×10^{-12}	4×10^{-7}	1.1×10^{-12}	$1\text{-}3\times10^{-10}$
V_t(V)	0.6	1.5	0.64	0.73	0.75	0.82	-0.34	-0.77	0.35
S (mV/dec)	102	166	90	105	100	95	150	135	70-80
DIBL (mV/V)	70	300	30	90	73	120	210	170	30-35

We propose that the improved performance of the frame gate architecture is due to its inherent immunity to plasma damage during gate polysilicon etch. In conventional vertical MOSFETS [3], the pillar top, bottom and sidewall are covered by a thin gate oxide. As a result, any over-etch of the polysilicon gate risks introducing dry etch damage at both the top and bottom of the pillar, thereby degrading the sub-threshold slope. In the FILOX process, the top and bottom of the pillar are protected by the thick FILOX oxide and hence this process should be more immune to dry etch damage. However, the results for the devices with single or double gate contacts in Fig.6 show degraded values of sub-threshold slope, suggesting the presence of dry etch damage. This result could be explained if the over-etch of the polysilicon gate was bigger than that of the nitride fillet (Fig.4), so that some gate oxide was exposed at the top of the pillar during the polysilicon gate etch. In the frame gate MOSFETs, the pillar sidewalls are protected by the polysilicon frame and hence there is no possibility of dry etch damage during polysilicon gate etch. The main disadvantage of the frame gate architecture is increased gate/source and gate/drain overlap capacitance where the polysilicon frame overlaps the top and bottom of the pillar. However, if the frame gate architecture is combined with the FILOX process, as in the current work, the thick FILOX oxide (typically 20 times thicker than the gate oxide) ensures that this increase in overlap capacitance is very small.

8 CONCLUSIONS

We have reported a CMOS compatible vertical MOSFET with a frame gate architecture that is suitable for RF applications, compatible with the FILOX process [5] and immune to dry etch damage. This architecture incorporates a thin polysilicon frame surrounding the pillar to aid the circulation of RF currents and to eliminate dry etch damage during polysilicon gate etch. The fabricated surround gate vertical MOSFETs with the frame gate architecture show no degradation of short channel effects when the channel length is scaled, while control devices show significantly degraded sub-threshold slope and DIBL. Frame gate transistors exhibit near ideal sub-threshold slopes of 70-80mV/decade and DIBL of 30-35mV/V for a 100 nm gate length nMOS device. In contrast control transistors without the frame gate exhibit sub-threshold slopes of 110 to 140 mV/decade and DIBL of 100 to 280 mV/V. The improved performance of short channel, frame gate vertical MOSFETs is attributed to their inherent immunity to dry etch damage.

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