Tunnel Barrier Properties in Polycrystalline-Si Single-Electron Transistors

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Abstract

This paper discusses the electrical and structural properties of tunnel barriers in polycrystalline-Si single-electron transistors. A novel point-contact device is introduced, which features an extremely short poly-Si nanowire as a channel. This structure suits for studying how a few discrete grain boundaries work as tunnel junctions. The relationship between tunnel barrier parameters and Coulomb blockade characteristics is investigated by comparing as-prepared and oxidized devices.

1. Introduction

Single electron transistors (SETs) have intensively been studied as one of possible alternative devices for the future VLSI technology since very low power consumption is expected. Several fabrication techniques have been reported for forming nanometer-scale electron islands in silicon-based materials. The most straightforward approach is to define a quantum dot by using electron beam lithography. A pattern-dependent oxidation (PADOX) method is one of reliable techniques to realize a well-defined silicon dot [1]. Another approach is to utilize electron islands naturally formed within patterned silicon nanostructures. It is known that a heavily doped silicon nanowire (NW) with a few tens nanometer in width shows clear Coulomb blockade (CB) phenomena due to 'natural' electron islands caused by randomly distributed dopant atoms. The heavily doped Si NW has often been used as a building block for making CB memories. The other method that also relies on naturally formed structures is to use an ultra thin polycrystalline-silicon (poly-Si) film [2]. It has been demonstrated that both a nanoscale memory node and a sensing channel can naturally be formed together in the poly-Si NW. In the poly-Si, silicon grains and grain boundaries (GBs) between adjacent islands act as electron islands and tunnel junctions (TJs), respectively. Along the GB an electrostatic potential barrier is formed by carries captured by trap levels in the band gap. The size of silicon grains can be controlled to some extent via a film thickness and/or process conditions for crystallization, and so the poly-Si nanostructures may enable us to go beyond the limit of lithography for realizing 'tailored' electron islands.

Apparently macroscopic properties of the poly-Si film have widely been studied for applications such as thin film transistors (TFTs) and static random access memories (SRAMs), and various techniques have been established to control the grain size and to improve carrier mobility by optimizing passivation conditions. However, microscopic properties of individual GBs have not been studied in detail, and there has been no clear guideline to optimize the GB-TJs for high-temperature SET operation. In this work, we examine the effects of oxidation on structural and electrical properties of the individual GB-TJs by using poly-Si point-contact transistors (PC-Trs). In addition, we examine the relationship between properties of GB-TJs and the CB characteristics of the PC-Trs.

2. Fabrication of poly-Si PC-Trs

To characterize individual GBs as a TJ, we fabricated nanometer-scale PC-Trs where the channel length and width are as small as the grain size or even smaller. Figure 1 shows a SEM image of a fabricated PC-Tr. The PC-Trs were fabricated in a 50 nm-thick solid-phase-crystallized (SPC) poly-Si film: a process flow is shown in Fig. 2. The inset of Fig. 1 is a SEM image of a Secco-etched poly-Si film that shows the grain size ranges from 20 nm to 150 nm. The PC-Trs with the channel width and length from 30 nm to 50 nm were patterned by a high-resolution e-beam lithography system and electrically isolated by RIE. The channel of the PC-Trs is therefore expected to contain only one or two grains at most [3].

We fabricated more than 60 PC-Trs using the same process. As shown in Fig. 2, half of the PC-Trs were then oxidized at 1000 ^{o}C for 15 min in dry O_2 ambient.

The rest of the PC-Trs were kept as a reference in order to study the oxidation effect on structural and electrical properties of the GB-TJs.

Electrical characterizations were performed for both as-prepared and oxidized PC-Trs at a temperature down to 4.2K. An effective potential barrier height qV_B of GBs was extracted from a temperature dependence of I_{ds}-V_{ds} characteristics at between 200K and 300K using the thermionic emission model [4]. Structural characterizations were also conducted by using TEM and SEM.

3. Results and Discussion

Figures 3(a) and (b) show I_{ds}-V_{ds} characteristics for as-prepared PC-Trs. The CB effect was not observed for any of the as-prepared PC-Trs measured at 4.2K. We observed nonlinear I_{ds}-V_{ds} characteristics associated with electron thermionic emission current over GBs for approximately one third of the as-prepared PC-Trs. The others showed linear I_{ds}-V_{ds} characteristics. Since the channel dimension is extremely small, the I_{ds}-V_{ds} characteristics in the PC-Trs are dominated by the electrical property of the narrow channel. Therefore, the as-prepared PC-Trs with the nonlinear I_{ds}-V_{ds} characteristics would contain a few GBs with a relatively high potential barrier, while those with linear I_{ds}-V_{ds} characteristics would have either no GB or few GBs with a very low potential barrier.

On contrast, most of the oxidized PC-Trs show a clear conductance oscillation associated with the CB effect. Figures 4(a) and (b) show typical I_{ds}-V_{gs} characteristics for the oxidized PC-Trs measured at 5K. We found that the CB characteristics for the oxidized PC-Trs can be classified into two groups: the characteristic with a Coulomb gap $V_T < 5$ meV and that with $V_T > 5$ meV. The conductance oscillation periods were quite similar among the PC-Trs with the same channel dimensions and $V_T < 5$ meV. On the other hand, the oscillation periods differ largely among the oxidized PC-Trs with $V_T > 5$ meV. Peak-to-valley (P/V) current ratios and tunnel resistances obtained for the PC-Trs with $V_T > 5$ meV were generally much larger than those with $V_T < 5$ meV.

Figures 5(a) and (b) show TEM images of the as-prepared and the oxidized poly-Si films. The both poly-Si films consist of columnar-shaped grains. Temperature dependences of resistance are shown in Fig. 6. Regarding the as-prepared PC-Trs, although each GB and grain may act as a tunnel barrier and an electron island, the estimated tunnel capacitance is larger than 80 aF because of the tall columnar grains (See the inset of Fig. 1 and Fig. 5(a)). Also the tunnel resistance estimated for the as-prepared PC-Trs is just as large as the quantum resistance R_Q of 25.6 kΩ. Therefore, for the as-prepared PC-Trs, both the electron charging energy and the tunnel resistance are not sufficiently large to observe the CB effect even at a cryogenic temperature. On contract, in the oxidized PC-Trs, the poly-Si film thickness decreases down to approximately 18 nm after the oxidation process [5]. The reduction of a film thickness leads to a decrease in a tunnel capacitance and consequently increases in the charging energy. In addition, the tunnel resistance is increased by more than two orders of magnitude after the oxidation treatment. (See Fig. 6). Both the increased charging energy and tunnel resistance result in the appearance of the CB effect.

Figure 7 presents the distributions of qV_B obtained for (a) the as-prepared and (b) the oxidized PC-Trs. It is found that the mean qV_B slightly increases after the oxidation process. We first like to note that the oxidized PC-Trs with $V_T < 5$ meV show a narrow distribution of qV_B (white bars in Fig. 7(b)) which resembles that for the as-prepared linear I_{ds}-V_{ds} PC-Trs (white bars in Fig. 7(a)). On the other hand, qV_B for the oxidized PC-Trs with $V_T > 5$meV spreads widely (dark gray bars in Fig. 7(b)), corresponding to the distribution of qV_B for the as-prepared PC-Trs with the nonlinear I_{ds}-V_{ds} (dark gray bars in Fig. 7(a)). These distributions represent unoxidized and oxidized GBs in the channel, and qV_B can vary a lot depending on the number and configuration of GBs in the individual devices.

As discussed earlier, it is thought for the as-prepared PC-Trs with the linear I_{ds}-V_{ds} characteristics that the device was formed on a grain larger than the size of its NW channel and there is no GB in the channel that affects the electron transport. All the GBs are contained in the large contact regions and would only show their averaged potential barrier heights. In these circumstances, the lengthy GBs in the contact regions are not oxidized entirely. Another possibility is that there exist some GBs in the NW channel that do not have many defect states and therefore do not form high potential barriers. The oxidation speed along such less defective GBs is not so fast and so does not have a large effect on their barrier properties. On the other hand, the GBs with larger qV_B obtained for the as-prepared PC-Trs with the nonlinear I_{ds}-V_{ds} characteristics are thought to be highly defective. These GBs are oxidized effectively and converted to the suboxide tunnel barriers with relatively high barrier heights.

The GB tunnel barrier thickness was estimated for the oxidized PC-Trs using a tunneling current simulator based on the transfer-matrix method [6]. The tunnel barrier is assumed to be simply rectangular shaped with the barrier height obtained above. By comparing the observed tunnel resistance with the simulated one, the GB barrier thickness of approximately 3 - 4 nm was obtained for the PC-Trs with $V_T > 5$ meV. This is consistent with the high-resolution TEM observation that reveals that GBs were oxidized faster than crystalline grains and that some silicon suboxide layers are as thick as about 3 nm. This result also supports that the CB characteristics for the PC-Trs with $V_T > 5$ meV are determined by the selectively oxidized GBs in the channel.

Two-dimensional capacitance calculation [7] was also conducted to evaluate the size of the grain that acts as a charging island. By comparing with the observed V_T, the charging island size evaluated for the PC-Tr shown in Fig. 4(a) is about 30 nm. Similar values were also obtained for other PC-Trs with $V_T < 5$ meV. We believe that an electron island with two tunnel junctions in these devices is formed by the PADOX-mode oxidation [8]. This scenario is supported by the fact that the CB oscillation periods obtained for the these PC-Trs with $V_T < 5$ meV are quite uniform among the fabricated devices and also show a dependence on the channel length L: 0.57±0.1 V for L=30 nm and 0.18±0.04 V for L=40 nm. In contrast, the island size estimated for the PC-Tr shown in Fig. 4(b) is as small as about 10 nm. This result is also consistent with the above discussion that few GBs existing in the channel were oxidized, which form very small electron charging islands.

Figure 8 shows the Coulomb gaps and the P/V current ratios as a function of tunnel resistance obtained for the oxidized PC-Trs at 4.2K. It shows some trends that both the P/V current ratio and the Coulomb gap increase with increasing the tunnel resistance. It can be seen that the tunnel resistance larger than 1 MΩ is needed to obtain good P/V ratios. The larger Coulomb gap results from an increase in the tunnel resistance and a decrease in the tunnel capacitance due to the formation of thicker GB tunnel barriers with the oxidation process. For improving the CB characteristics of the poly-Si PC-Trs, the structural parameters of GBs, such as potential barrier height and thickness, could be optimized further through various oxidation, annealing and passivation treatment [9].

4. Conclusions

The electrical and structural characterization of GB-TJs has been performed for as-prepared and oxidized PC-Trs fabricated in a heavily doped poly-Si film. We have demonstrated that GBs selectively oxidized at 1000 ^{o}C for 15 min provide a tunnel resistance large enough to realize the CB effect. The maximum effective tunnel barrier height and barrier thickness of the oxidized GBs have been found to be 90 meV and approximately 4 nm, respectively.

5. Acknowledgement

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6. References

[1] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase and M. Tabe, *IEDM* 1994, p. 938.
[2] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai and K. Seki: *IEEE Trans. Electron Devices* **41** (1994) 1628.
[3] Y. Furuta, H. Mizuta, K. Nakazato, Y. T. Tan, T. Kamiya, Z. A. K. Durrani, H. Ahmed and K. Taniguchi, *Jpn. J. Appl. Phys.* **40** (2001) L615.
[4] J. Y. W. Seto, *J. Appl. Phys.* **46** (1975) 5247.
[5] Y. T. Tan, Z. A. K. Durrani and H. Ahmed, *J. Appl. Phys.* **89** (2001) 1262.
[6] H. Mizuta and T. Tanoue, *The Physics and Applications of Resonant Tunnelling Diodes* (Cambridge University Press, Cambridge, 1995) p. 15.
[7] O. -H. Müller, K. Katayama and H. Mizuta, *J. Appl. Phys.* **84** (1998) 5603.
[8] T. H. –H. Altebäumer, *The Physics and Characterisation of Bi-directional Electron Pump*, PhD Thesis 2002, University of Cambridge
[9] T. Kamiya, Y. T. Tan, Z. A. K. Durrani and H. Ahmed: to be published in *J. Non-Cryst. Solids* (2002).

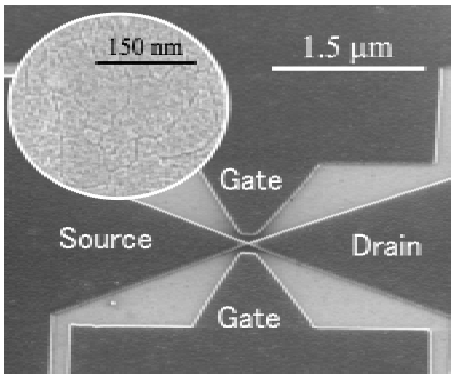

Figure 1. SEM image of an as-prepared PC-Tr with a channel 30-nm-wide and 30-nm-long. The inset figure shows the grain structure of Secco-etched poly-Si film.

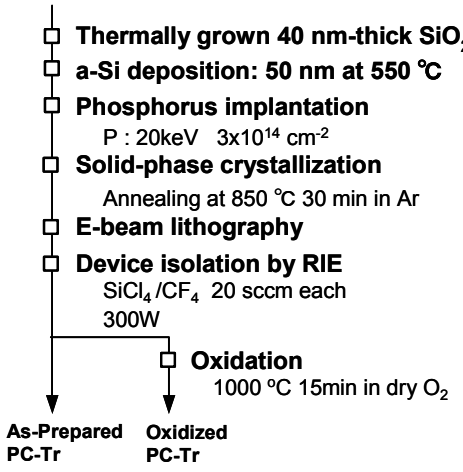

Figure 2. Fabrication sequence for PC-Trs.

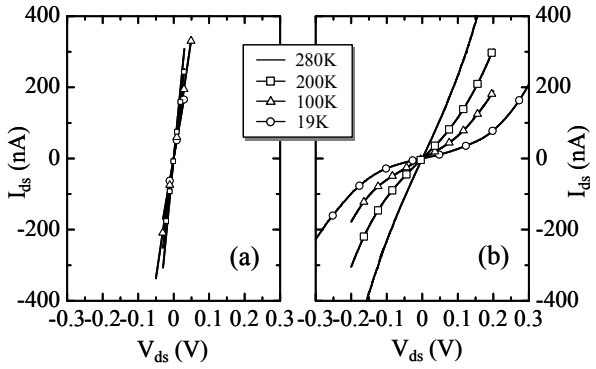

Figure 3. I_{ds}-V_{ds} characteristics of as-prepared PC-Trs with Width/Length = 40 nm/50 nm.

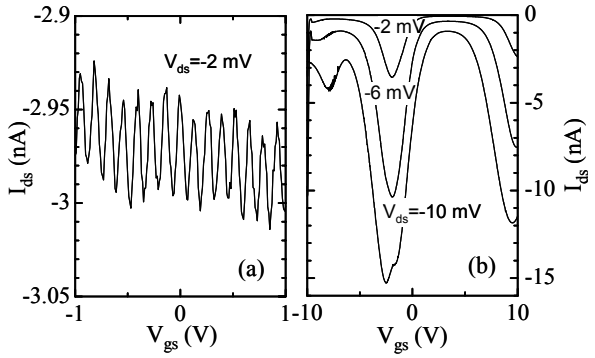

Figure 4. I_{ds}-V_{gs} characteristics of oxidized PC-Tr (a) with V_T < 5 meV (b) with V_T > 5 meV. Both oxidized PC-Trs clearly exhibited Coulomb blockade effects.

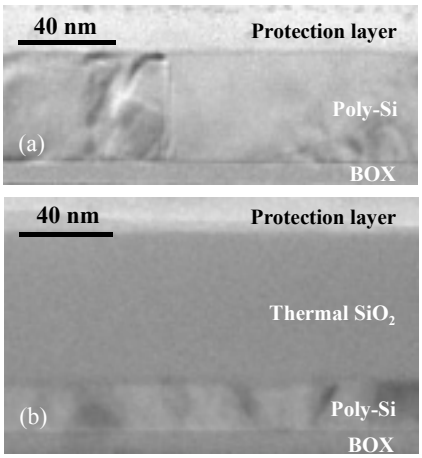

Figure 5. TEM images taken for as-prepared and oxidized poly-Si film. Film thickness is reduced to be approximately 18 nm after oxidation at 1000 °C for 15 min in dry O_2 ambient.

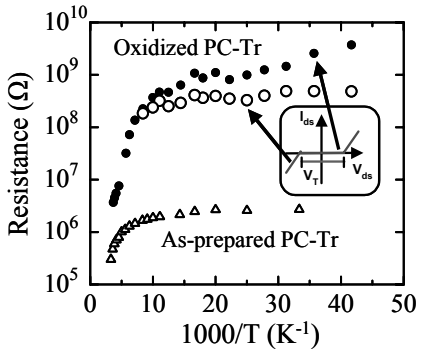

Figure 6. Temperature dependence of resistance obtained for the as-prepared PC-Tr in Fig. 3(b) and the oxidized PC-Tr in Fig. 4(b)

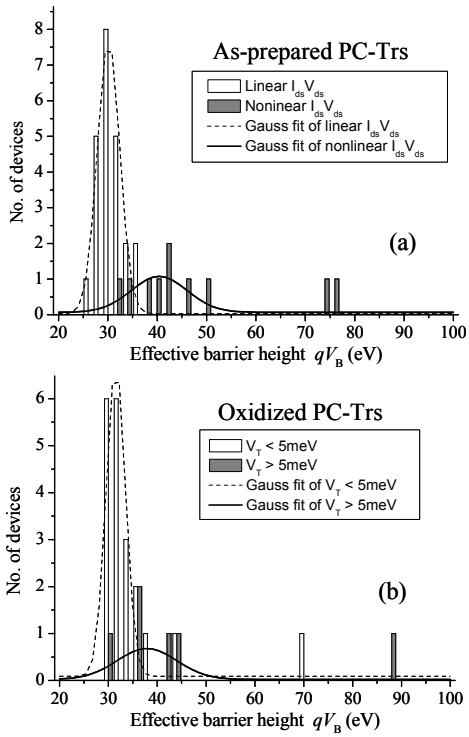

Figure 7. The distributions of qV_B for (a) as-prepared PC-Trs and (b) oxidized PC-Trs.

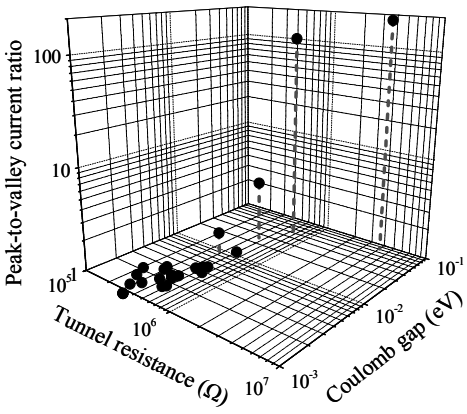

Figure 8. Coulomb gaps and Peak-to-valley current ratios as a function of tunnel resistance. All data were taken at 4.2K